Reference Schematics For RK3588S2

RK3588S2_Tablet_REF_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC or 2Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
4) ROM: eMMC5.1(Default) or SPI Falsh
5) Support: 1 x Micro SD Card3.0
6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
7) Support: 1 x 4Lanes MIPI D/CPHY RX Camera
8) Support: 4 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
10) Support: 2 x 4Lanes MIPI D/CPHY TX
11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
13) Support: 2 x PDM MIC Array
14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

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Project:	RK3588S2_Tablet_REF				
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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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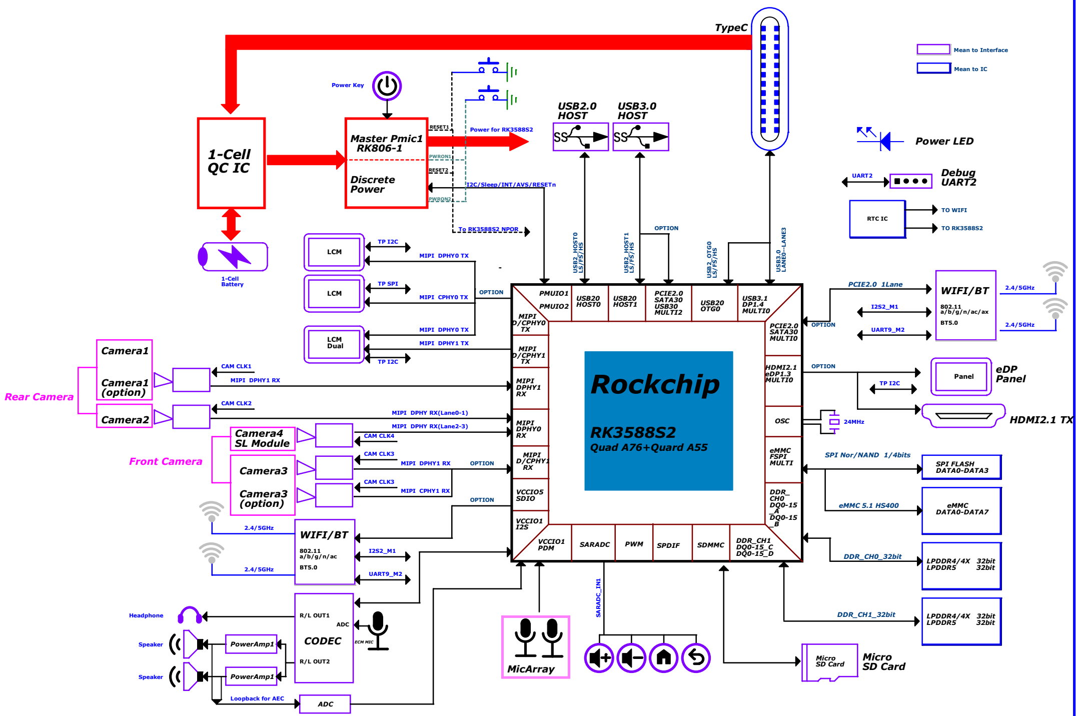
Revision History

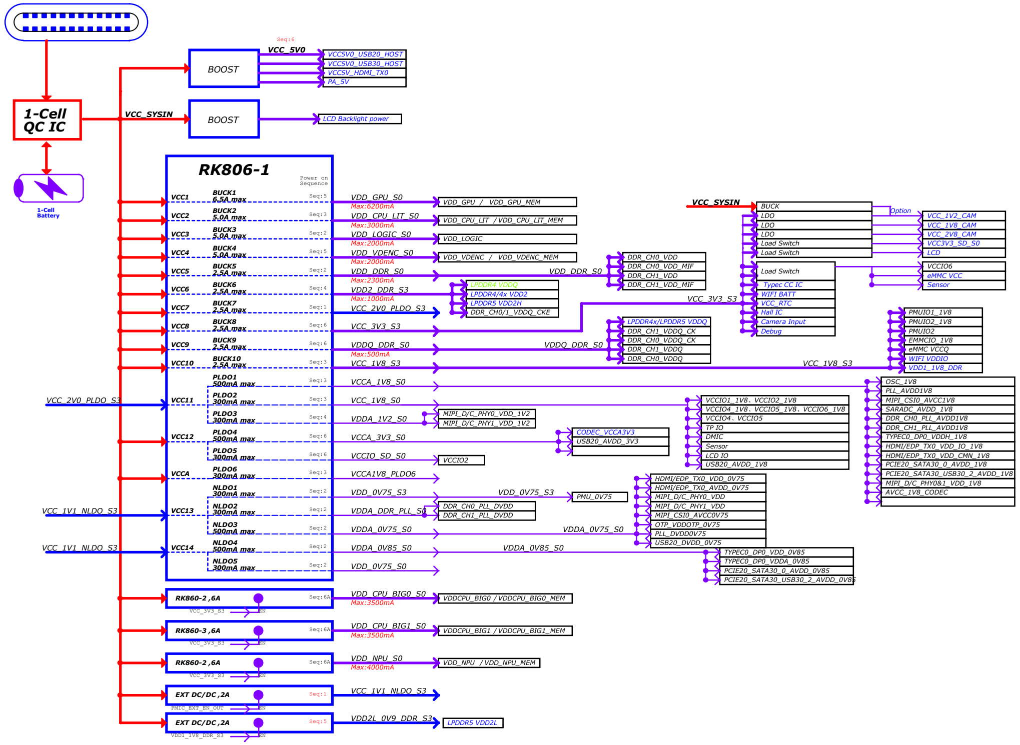
Version	Date	By	Change Dsecription	Approved
V1.0	2023-12-14	Joseph.Wei	1:Revision preliminary version	

RK3588S2 Tablet Ref Block Diagram for 1-Cell Charger



TypeC
Power Key
1-Cell QC IC
1-Cell Battery
Master Pmic1 RK806-1
Discrete Power
Power for RK3588S2
I2C/Sleep/INT/AVS/RESETn
USB2.0 HOST
USB3.0 HOST
Mean to Interface
Mean to IC
Power LED
Debug UART2
UART2
RTC IC
TO WIFI
TO RK3588S2
LCM
LCM
LCM Dual
TP I2C
TP SPI
MIPI DPHY0 TX
MIPI CPHY0 TX
MIPI DPHY1 TX
OPTION
Camera1
Camera1 (option)
Camera2
Rear Camera
CAM CLK1
CAM CLK2
MIPI DPHY1 RX
MIPI DPHY RX(Lane0-1)
MIPI DPHY RX(Lane2-3)
Camera4 SL Module
Camera3
Camera3 (option)
Front Camera
CAM CLK4
CAM CLK3
MIPI DPHY1 RX
MIPI CPHY1 RX
WIFI/BT
802.11 a/b/g/n/ac
BT5.0
2.4/5GHz
I2S2_M1
UART9_M2
Headphone
Speaker
PowerAmp1
CODEC
R/L OUT1
R/L OUT2
ADC
Loopback for AEC
MicArray
Rockchip
RK3588S2
Quad A76+Quard A55
PMUIO1
PMUIO2
USB20 HOST0
USB20 HOST1
PCIE2.0 SATA30 USB30 MULTI2
USB20 OTG0
USB3.1 DP1.4 MULTI0
PCIE2.0 SATA30 MULTI0
HDMI2.1 eDP1.3 MULTI0
OSC
eMMC FSPI MULTI
DDR_CH0 DQ0-15_A DQ0-15_B
DDR_CH1 DQ0-15_C DQ0-15_D
SDMMC
SPDIF
PWM
SARADC
VCCIO1 PDM
VCCIO1 I2S
VCCIO5 SDIO
MIPI D/CPHY0 TX
MIPI D/CPHY1 TX
MIPI DPHY1 RX
MIPI DPHY0 RX
MIPI D/CPHY1 RX
PCIE2.0 1Lane
WIFI/BT
802.11 a/b/g/n/ac/ax
BT5.0
I2S2_M1
UART9_M2
eDP Panel
Panel
TP I2C
HDMI2.1 TX
24MHz
SPI Nor/NAND 1/4bits
SPI FLASH DATA0-DATA3
eMMC 5.1 HS400
eMMC DATA0-DATA7
DDR_CH0_32bit
DDR_CH1_32bit
LPDDR4/4X 32bit
LPDDR5 32bit
Micro SD Card
SARADC_IN1

Power tree for 1-Cell Charger



1-Cell QC IC
1-Cell Battery
VCC_5V0
VCC_SYSIN
BOOST
VCC5V0_USB20_HOST
VCC5V0_USB30_HOST
VCC5V_HDMI_TX0
PA_5V
LCD Backlight power
RK806-1
VDD_GPU_S0
VDD_CPU_LIT_S0
VDD_LOGIC_S0
VDD_VDENC_S0
VDD_DDR_S0
VDD2_DDR_S3
VCC_2V0_PLDO_S3
VCC_3V3_S3
VDDQ_DDR_S0
VCC_1V8_S3
VCCA_1V8_S0
VCC_1V8_S0
VDDA_1V2_S0
VCCA_3V3_S0
VCCIO_SD_S0
VCCA1V8_PLDO6
VDD_0V75_S3
VDDA_DDR_PLL_S0
VDDA_0V75_S0
VDDA_0V85_S0
VDD_0V75_S0
RK860-2,6A
RK860-3,6A
EXT DC/DC,2A
VDD_CPU_BIG0_S0
VDD_CPU_BIG1_S0
VDD_NPU_S0
VCC_1V1_NLDO_S3
VDD2L_0V9_DDR_S3
VDD_GPU / VDD_GPU_MEM
VDD_CPU_LIT / VDD_CPU_LIT_MEM
VDD_LOGIC
VDD_VDENC / VDD_VDENC_MEM
DDR_CH0_VDD
DDR_CH0_VDD_MIF
DDR_CH1_VDD
DDR_CH1_VDD_MIF
LPDDR4/4x VDD2
LPDDR5 VDD2H
DDR_CH0/1_VDDQ_CKE
LPDDR4x/LPDDR5 VDDQ
VDDCPU_BIG0 / VDDCPU_BIG0_MEM
VDDCPU_BIG1 / VDDCPU_BIG1_MEM
VDD_NPU / VDD_NPU_MEM
LPDDR5 VDD2L
VCC_SYSIN
BUCK
LDO
Load Switch
VCC_1V2_CAM
VCC_1V8_CAM
VCC_2V8_CAM
VCC3V3_SD_S0
LCD
VCCIO6
eMMC VCC
Sensor
Type CC IC
WIFI BATT
VCC_RTC
Hall IC
Camera Input
Debug
PMUIO1_1V8
PMUIO2_1V8
PMUIO2
EMMCIO_1V8
eMMC VCCQ
WIFI VDDIO
VDD1_1V8_DDR
OSC_1V8
PLL_AVDD1V8
MIPI_CSI0_AVCC1V8
SARADC_AVDD_1V8
DDR_CH0_PLL_AVDD1V8
DDR_CH1_PLL_AVDD1V8
TYPEC0_DP0_VDDH_1V8
HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8
PCIE20_SATA30_0_AVDD_1V8
PCIE20_SATA30_USB30_2_AVDD_1V8
MIPI_D/C_PHY0&1_VDD_1V8
AVCC_1V8_CODEC
VCCIO1_1V8、VCCIO2_1V8
VCCIO4_1V8、VCCIO5_1V8、VCCIO6_1V8
VCCIO4、VCCIO5
TP IO
DMIC
Sensor
LCD IO
USB20_AVDD_1V8
MIPI_D/C_PHY0_VDD_1V2
MIPI_D/C_PHY1_VDD_1V2
CODEC_VCCA3V3
USB20_AVDD_3V3
VCCIO2
PMU_0V75
DDR_CH0_PLL_DVDD
DDR_CH1_PLL_DVDD
HDMI/EDP_TX0_VDD_0V75
HDMI/EDP_TX0_AVDD_0V75
MIPI_D/C_PHY0_VDD
MIPI_D/C_PHY1_VDD
MIPI_CSI0_AVCC0V75
OTP_VDDOTP_0V75
PLL_DVDD0V75
USB20_DVDD_0V75
TYPEC0_DP0_VDD_0V85
TYPEC0_DP0_VDDA_0V85
PCIE20_SATA30_0_AVDD_0V85
PCIE20_SATA30_USB30_2_AVDD_0V85

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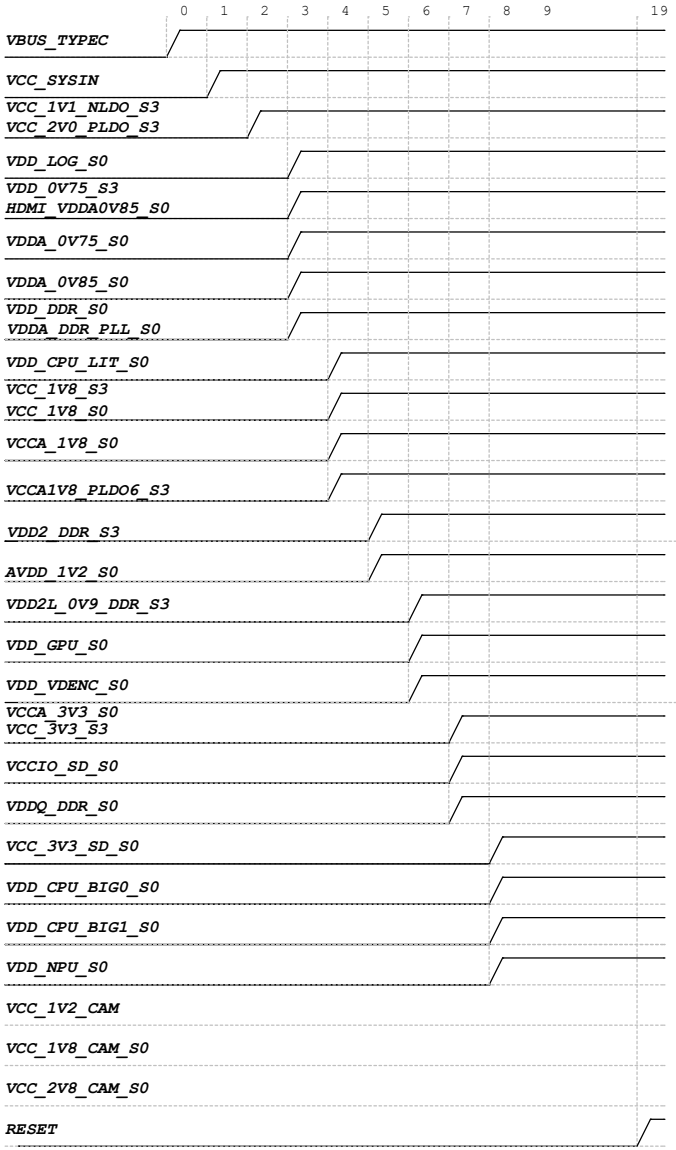
Project: RK3588S2_Tablet_REF
File: 03.Block Diagram_PowerTree-1cell

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	HDMI_VDDA0V85_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.8V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.8V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.8V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

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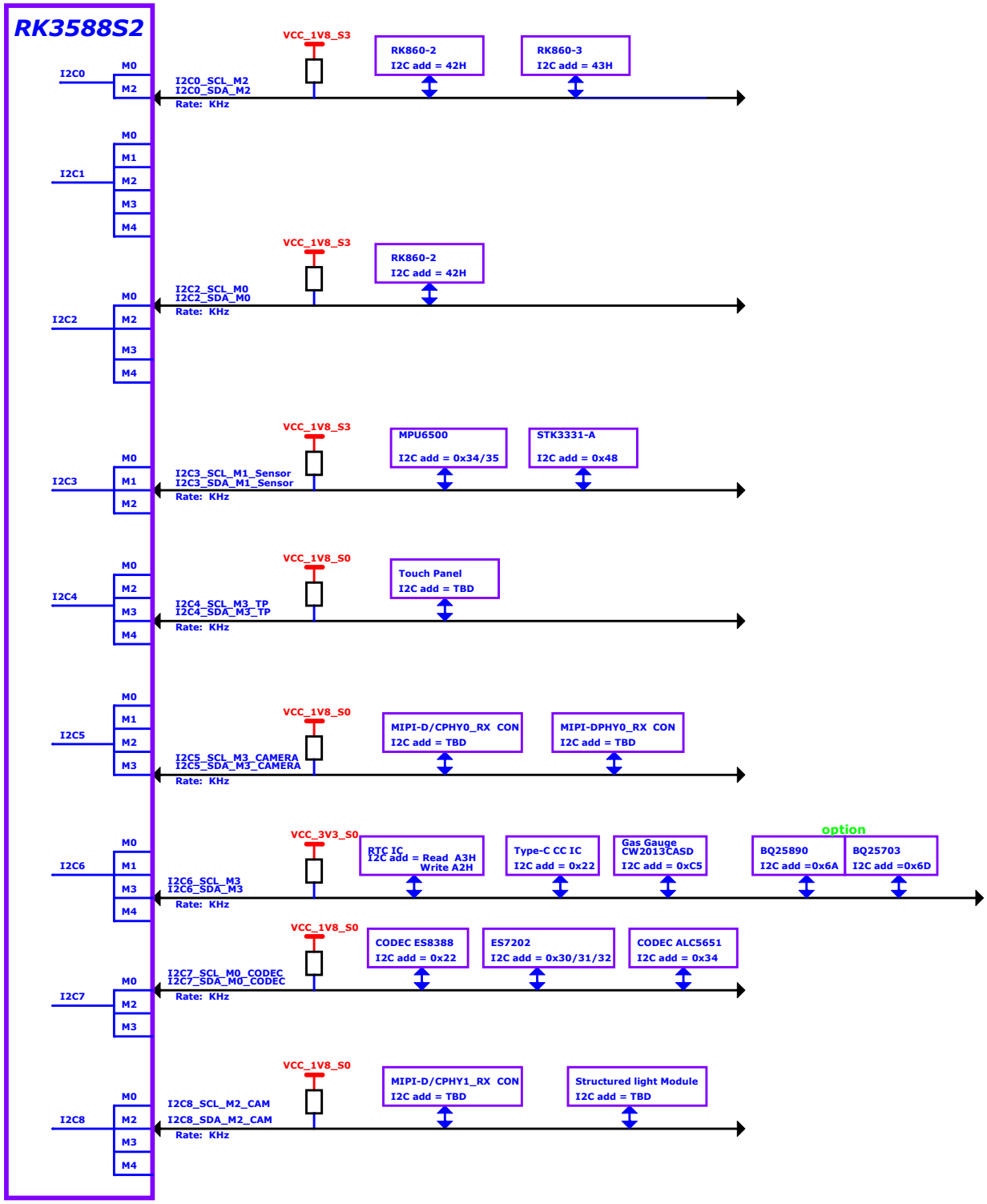
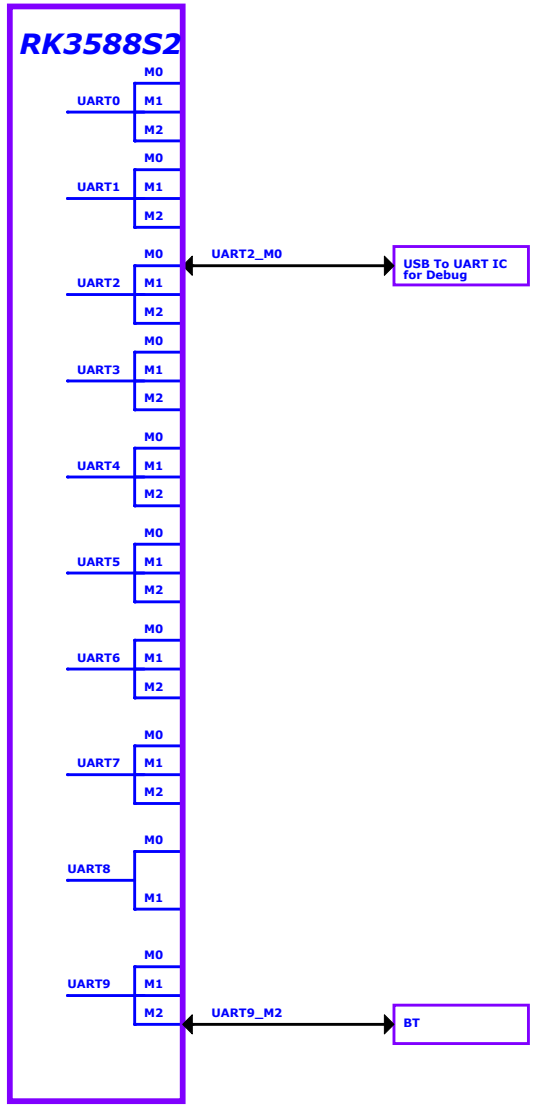
I2C MAP



UART MAP



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S2_Tablet_REF
File:	06.Lower-Speed Bus Map
Date:	Monday, October 13, 2025
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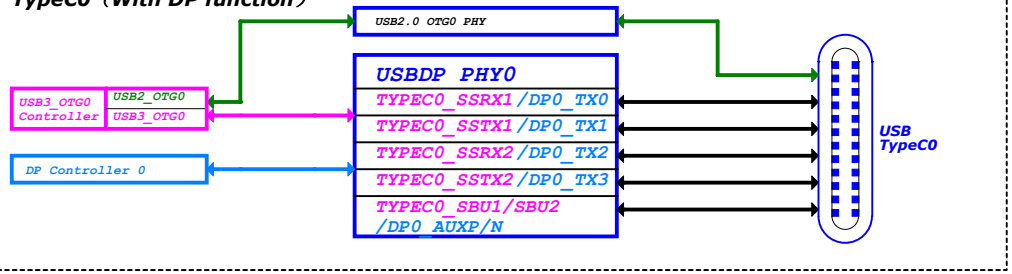
USB Controller Configure Table

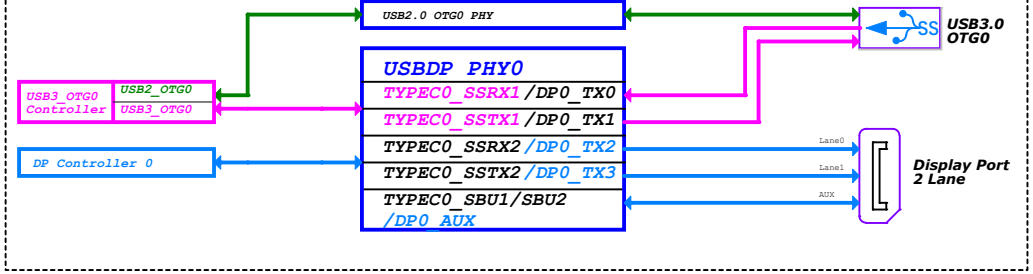
Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1M/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2M/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2M	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

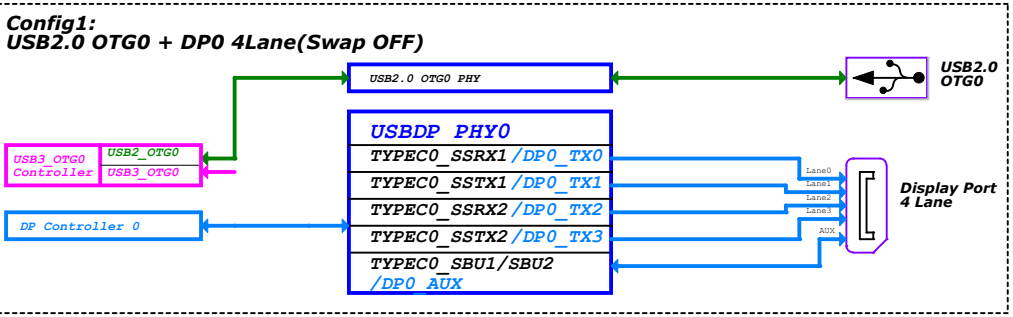
Config0:
TypeC0（With DP function）



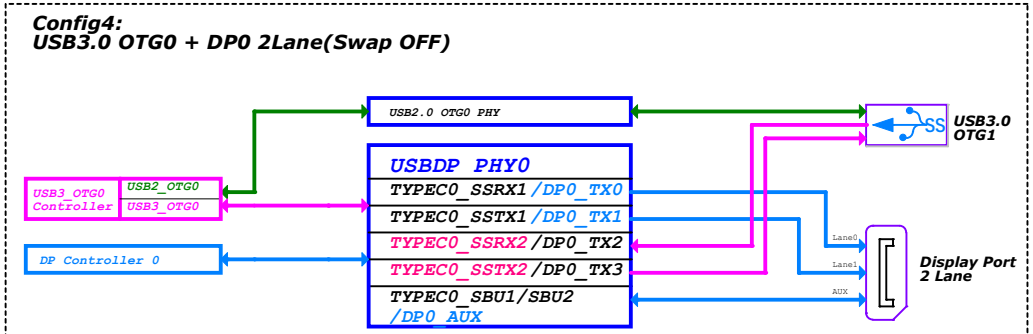
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



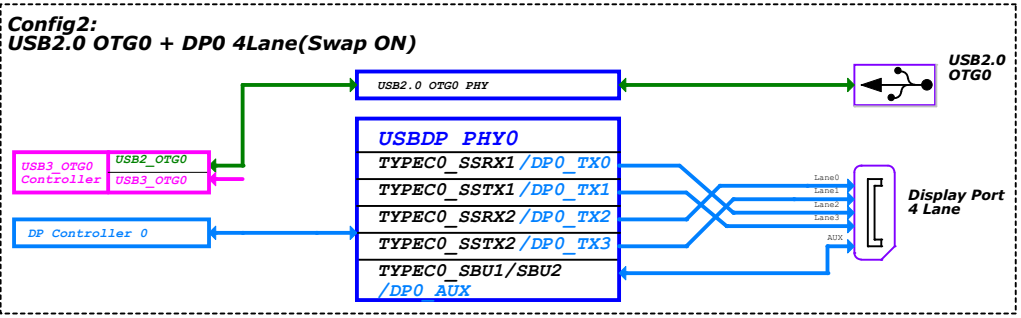
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S2_Tablet_REF
File:	07.USB Controller Configure Tab
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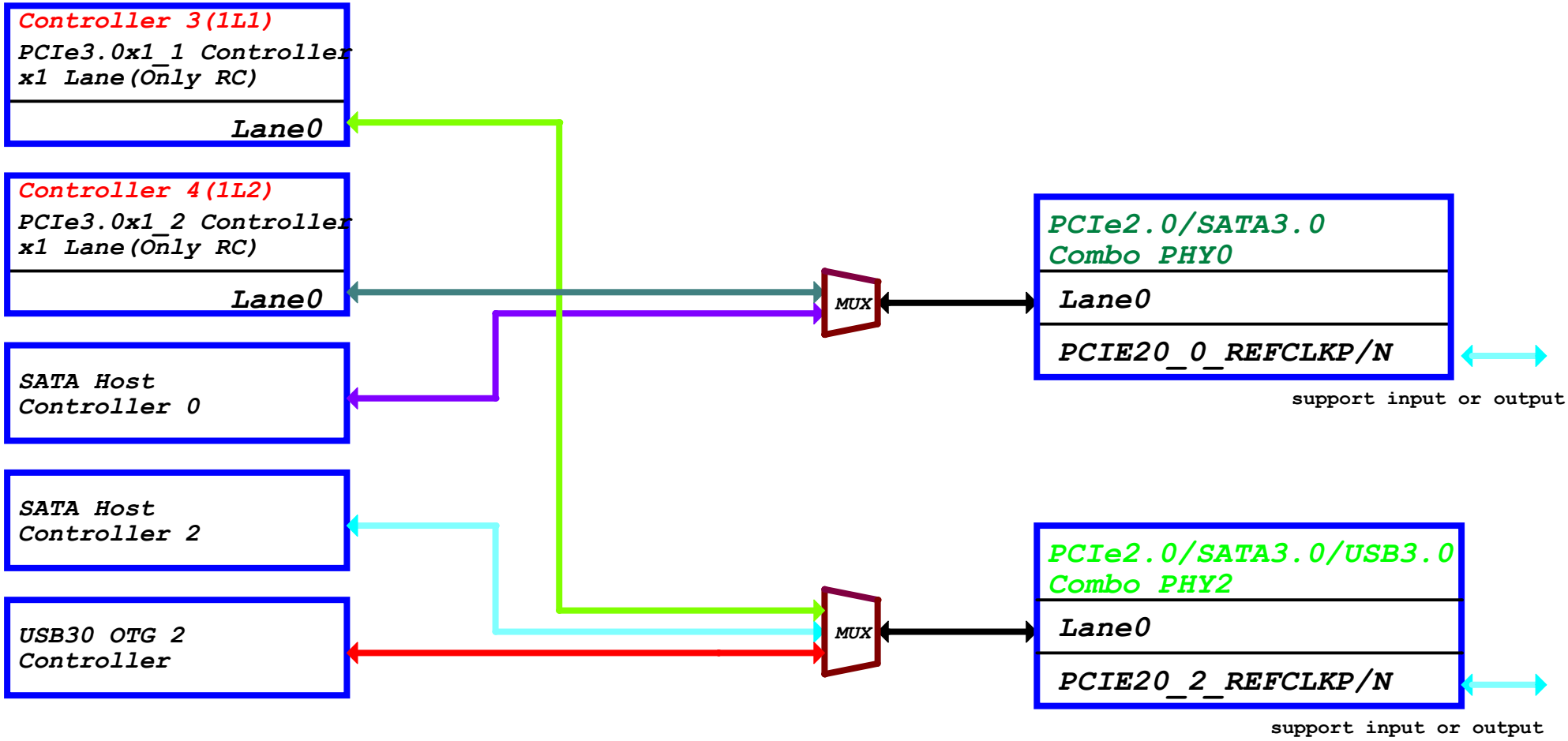
Sheet:	8 of 35

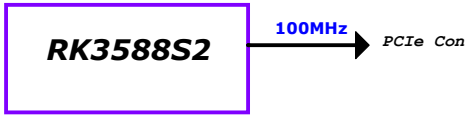
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK

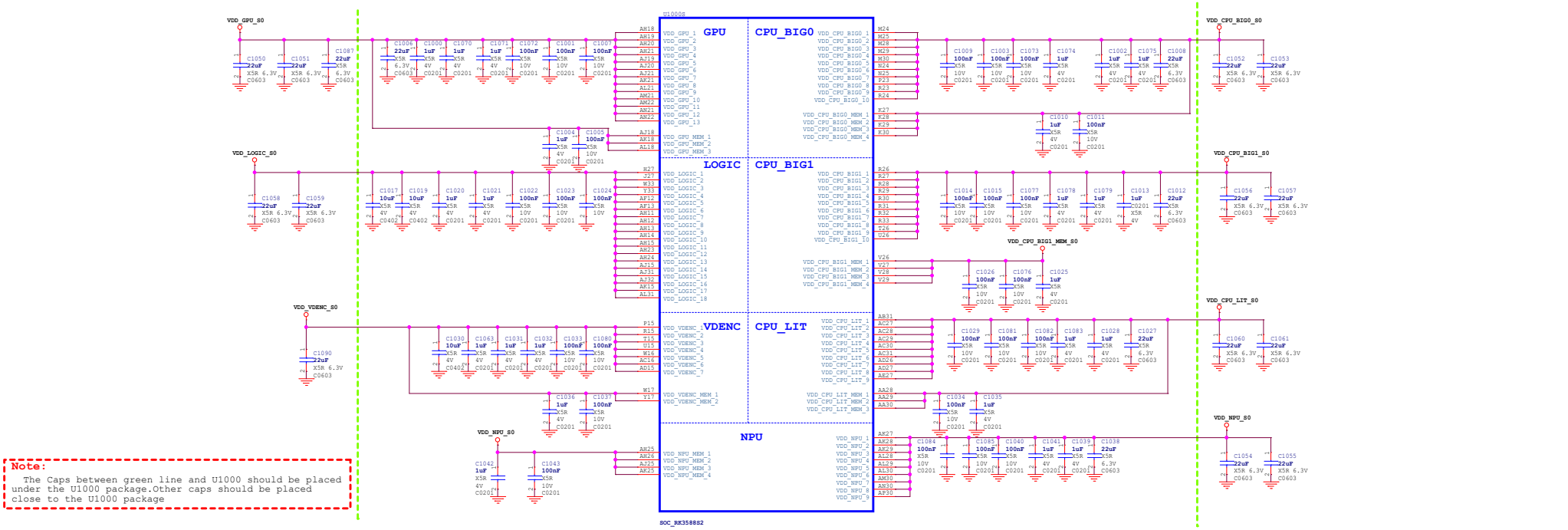


Note:

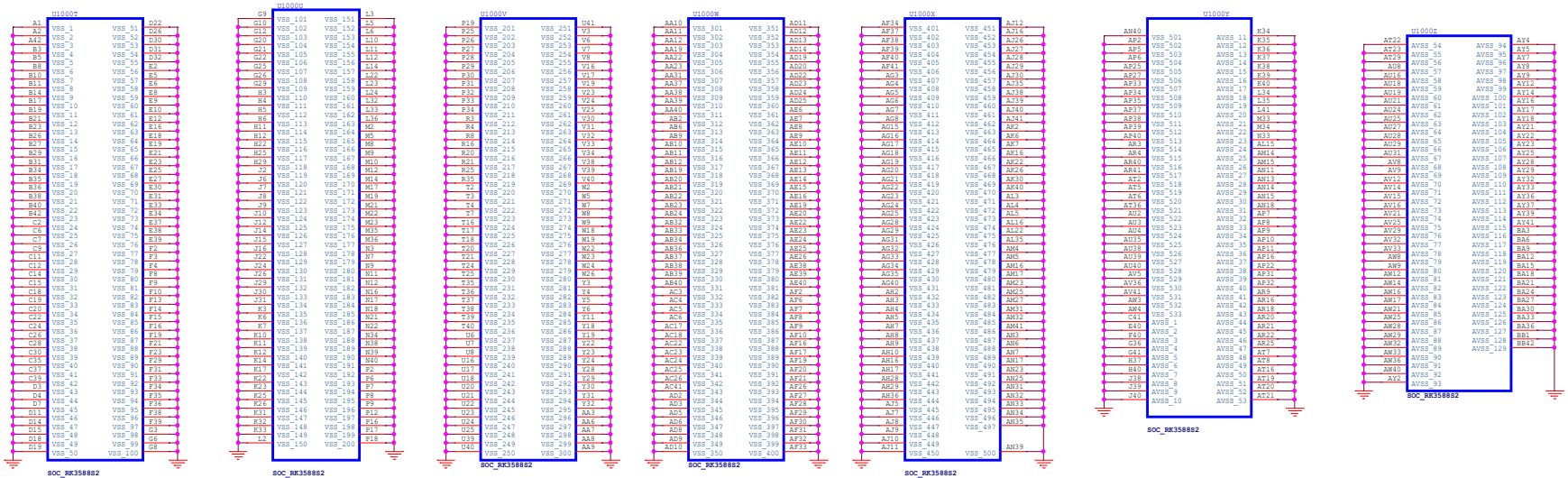
PCIE20_*_REFCLKP/N is output or input gpio
M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S2_Tablet_REF				
File:	08.PCIE Fun Map				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	9 of 53

RK3588S2 (Power&Gnd)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



Rockchip Confidential

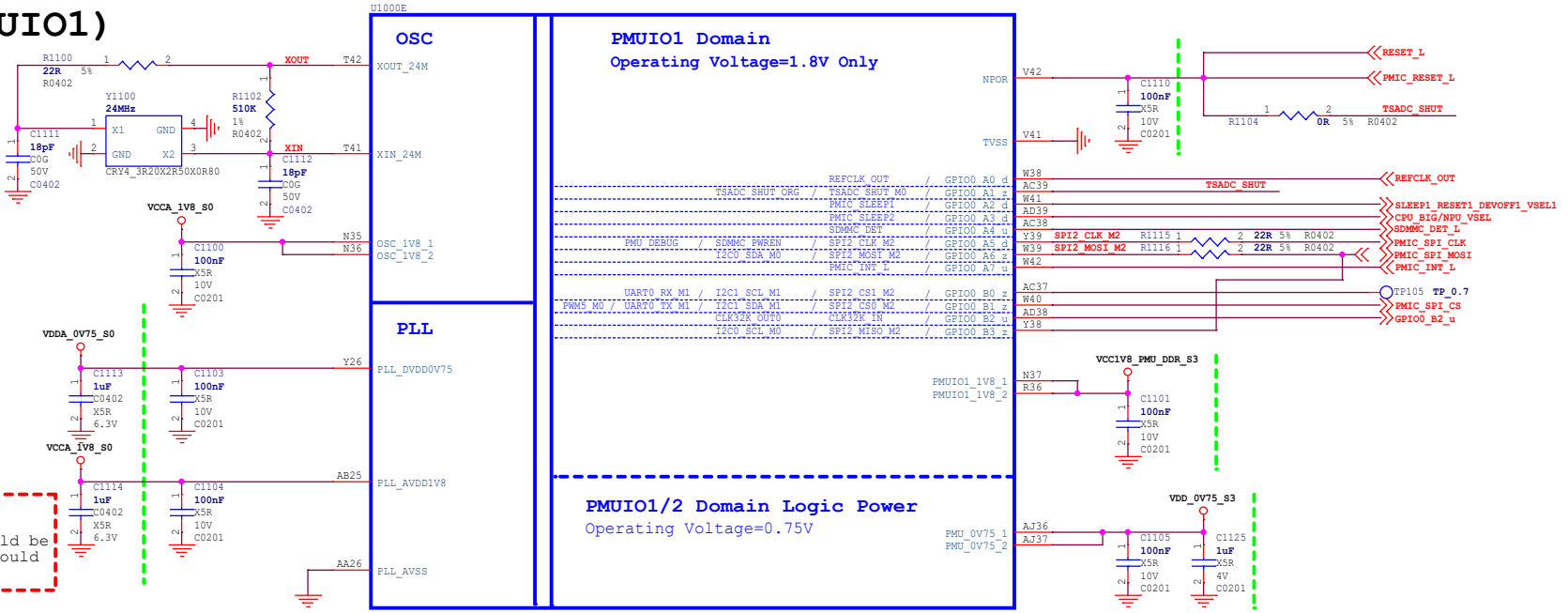
Rockchip Electronics Co., Ltd			
Project:	RK3588S2_Tablet_REF		
File:	10.RK3588S2_Power/GND		
Date:	Monday, October 13, 2025	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet:	10 of 53

RK3588S2 (OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

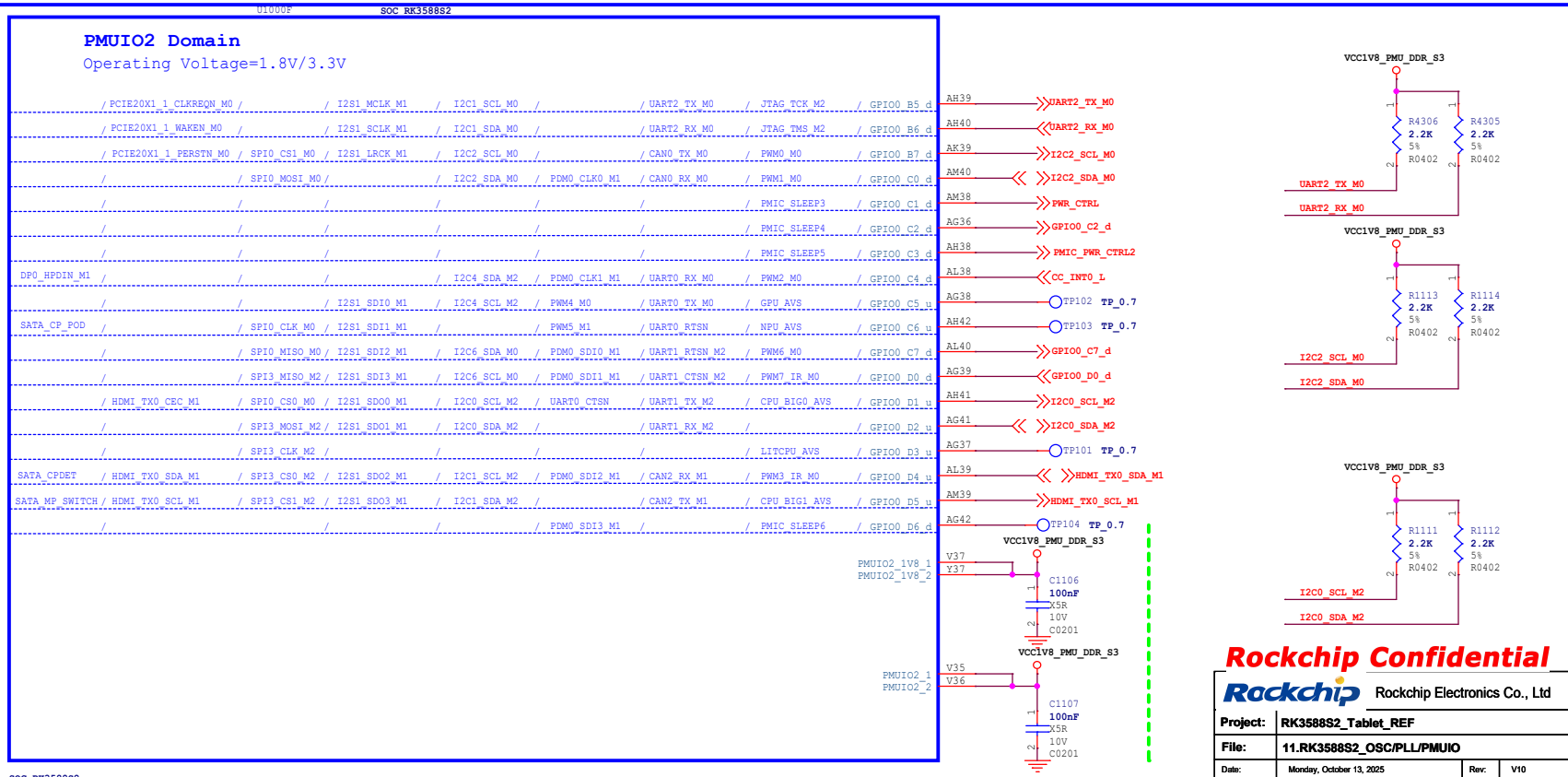
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588S2 (PMUIO2)

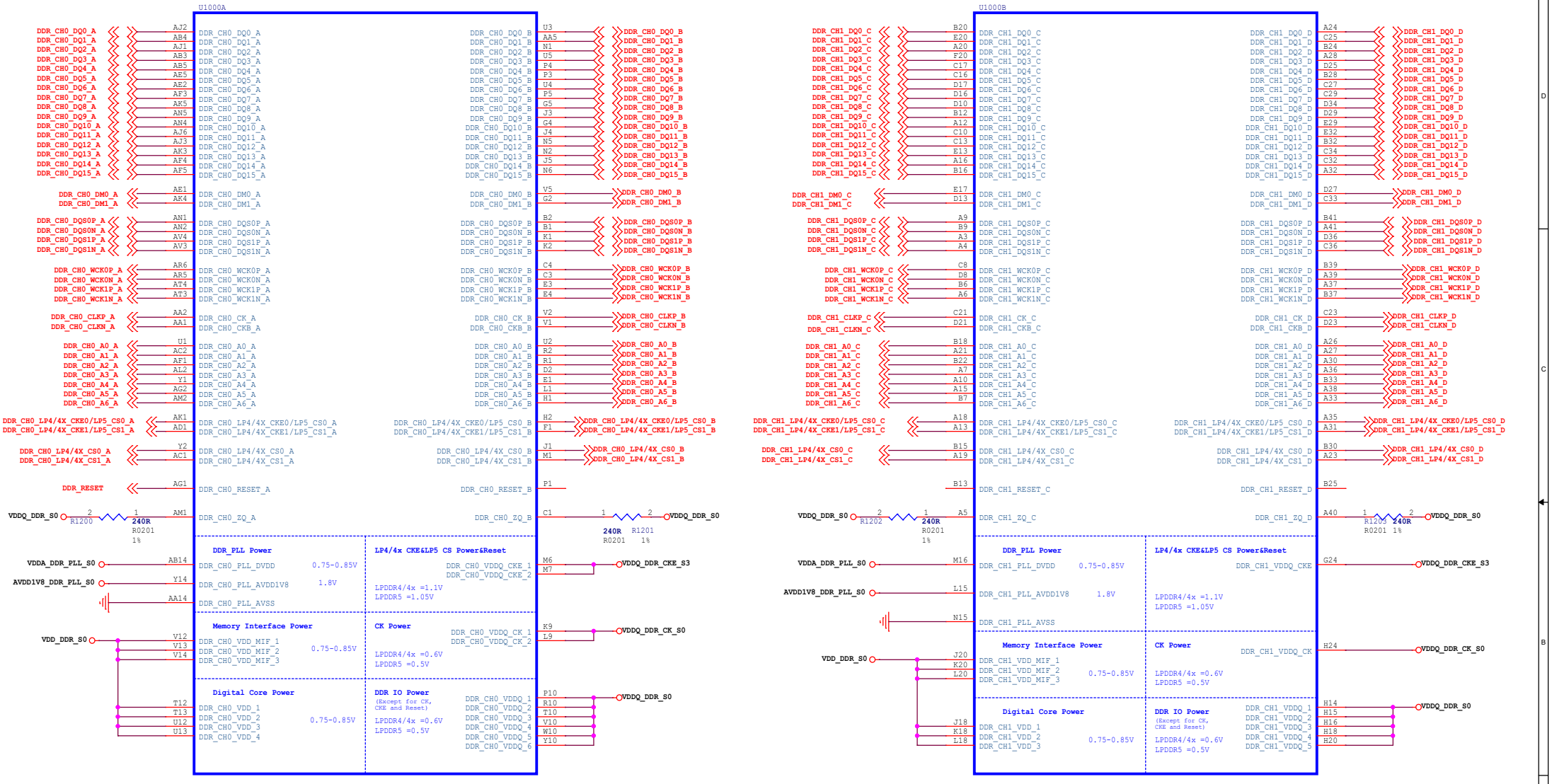


SOC_RK3588S2

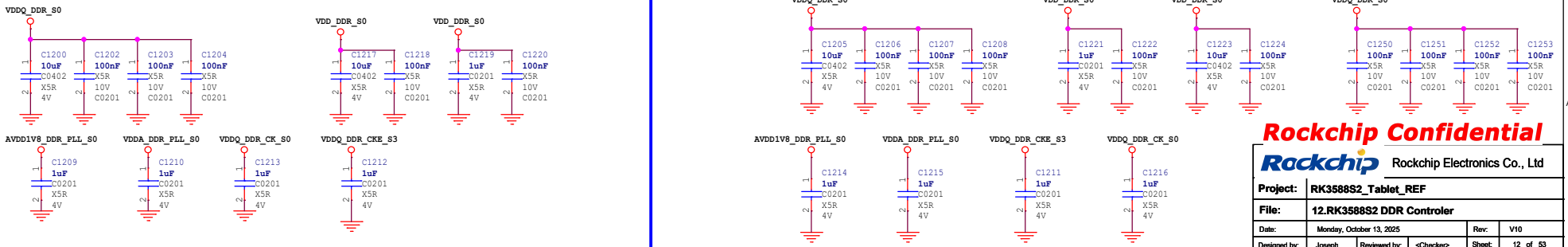
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	11.RK3588S2_OSC/PLL/PMUIO				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	11 of 53

RK3588S2 (DDR PHY)



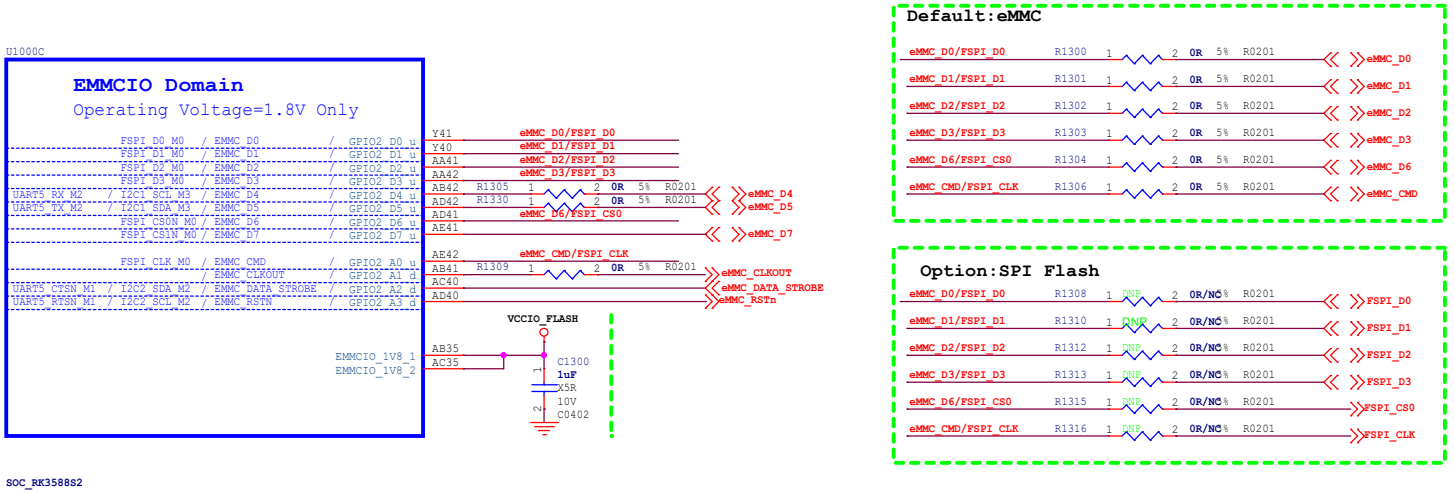
DDR FILTER



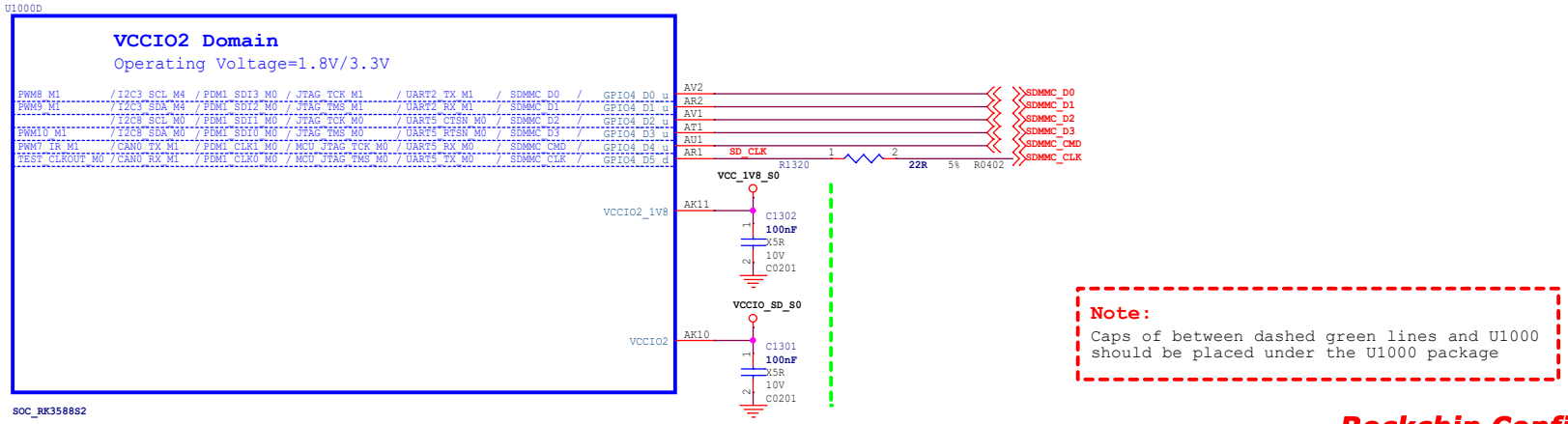
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	12.RK3588S2 DDR Controler				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	12 of 53

RK3588S2(EMMCIO Domain)



RK3588S2(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

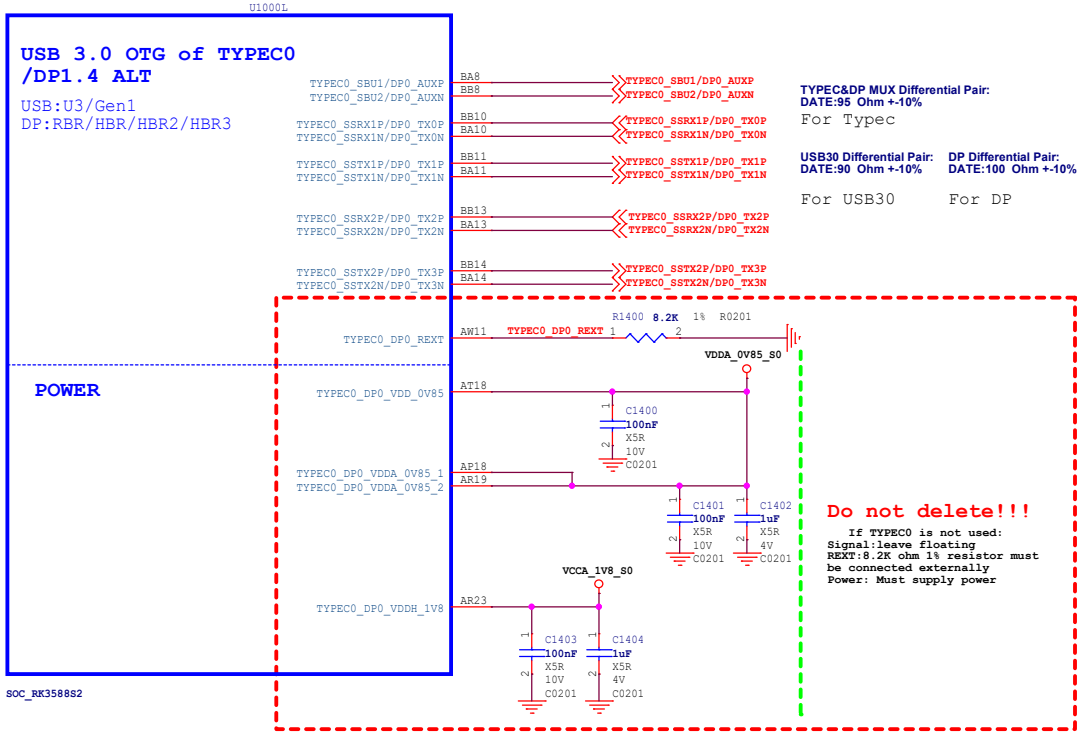
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S2_Tablet_REF				
File:	13.RK3588S2 Flash/SD Controller				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	13 of 53

RK3588S2(USB3.0/DP1.4)

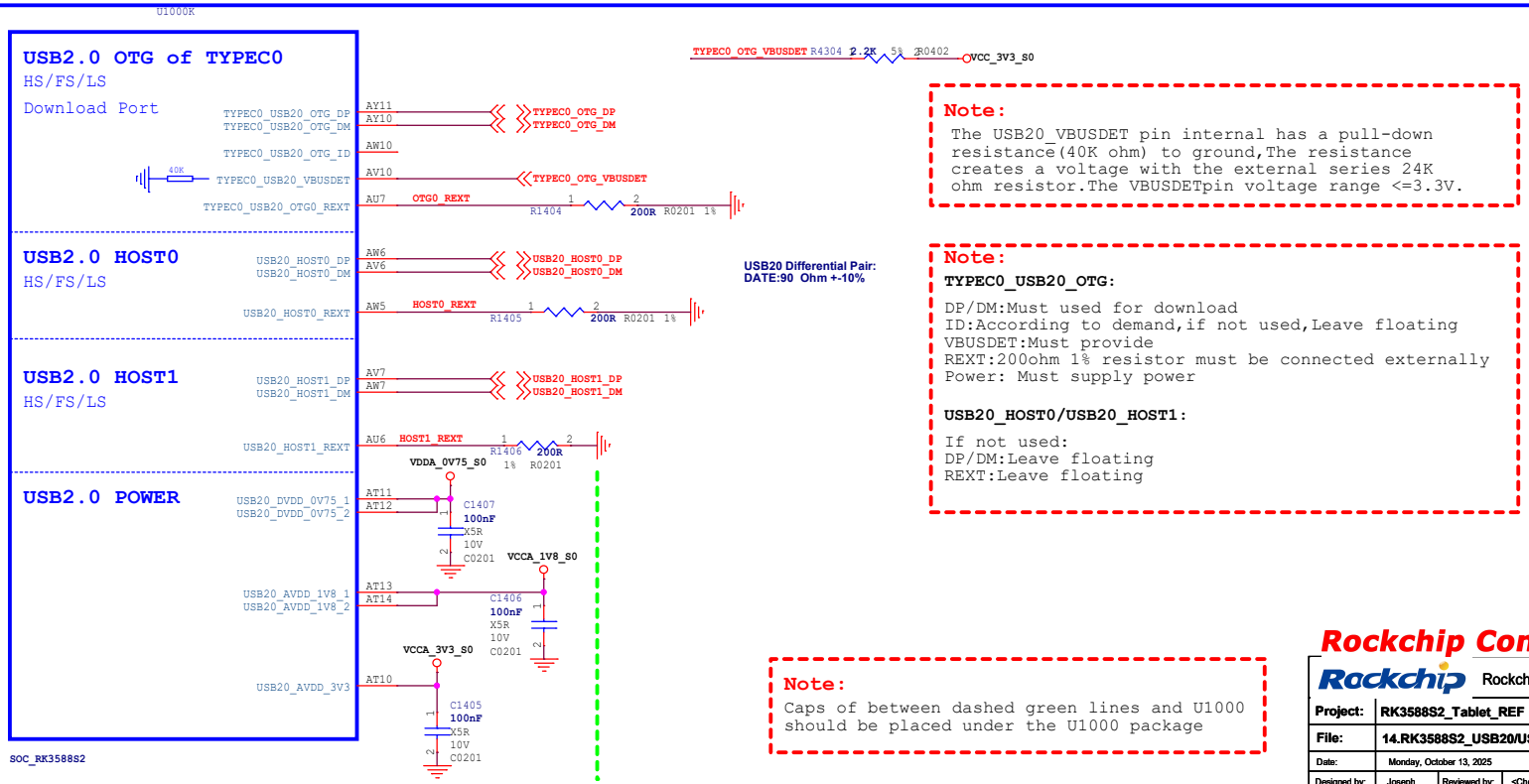
USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

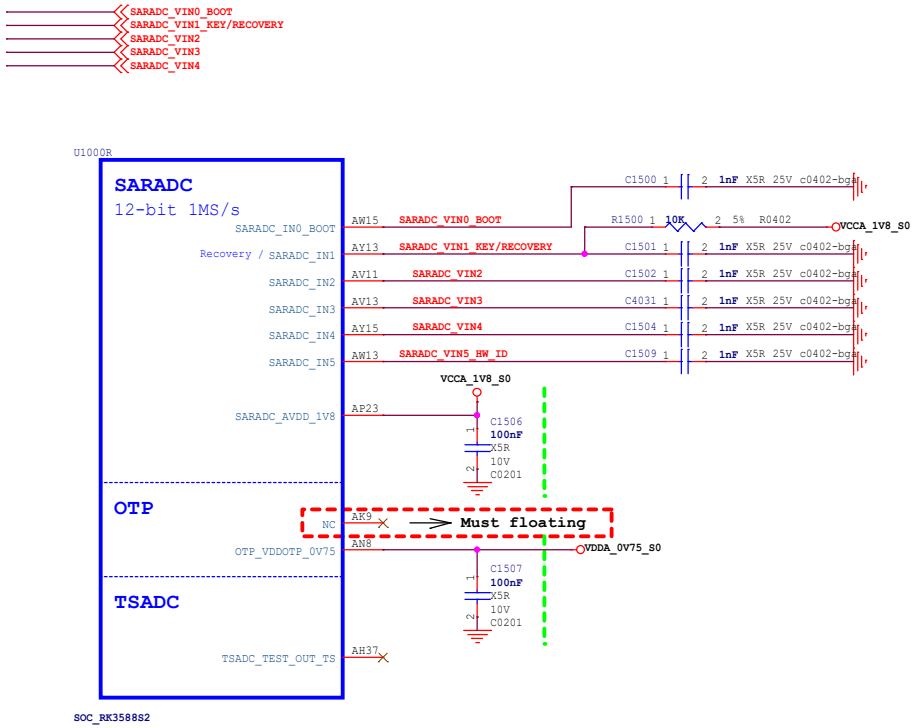


RK3588S2(USB2.0)

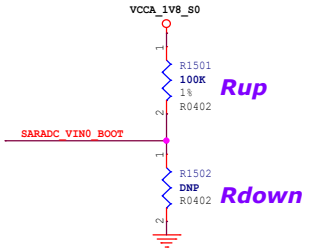


Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	14.RK3588S2_USB20/USB30/DP PHY				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	14 of 53

RK3588S2 (SARADC/OTP/TSADC)

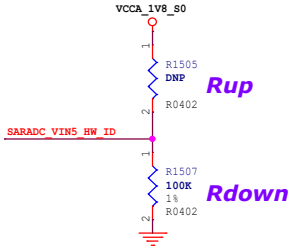


BOOT MODE CONFIG



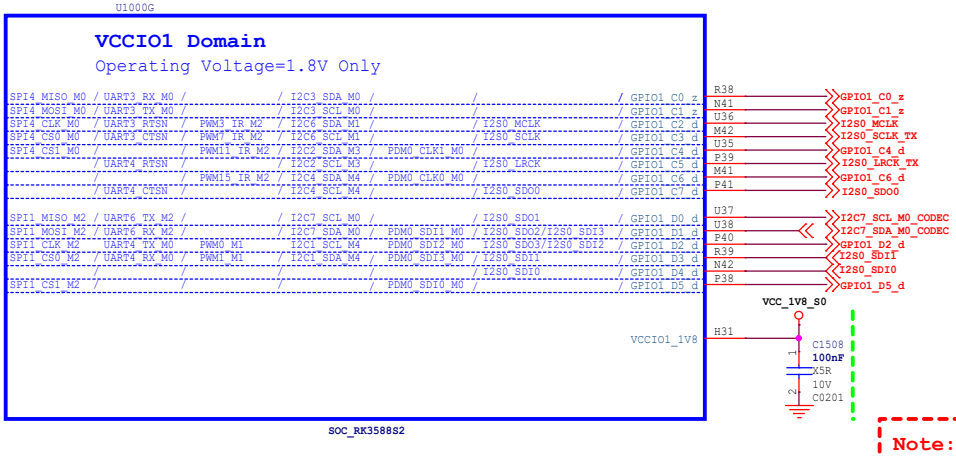
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

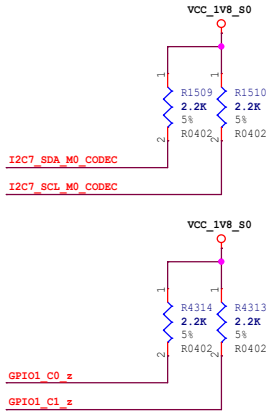
BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S2 (VCCIO1 Domain)

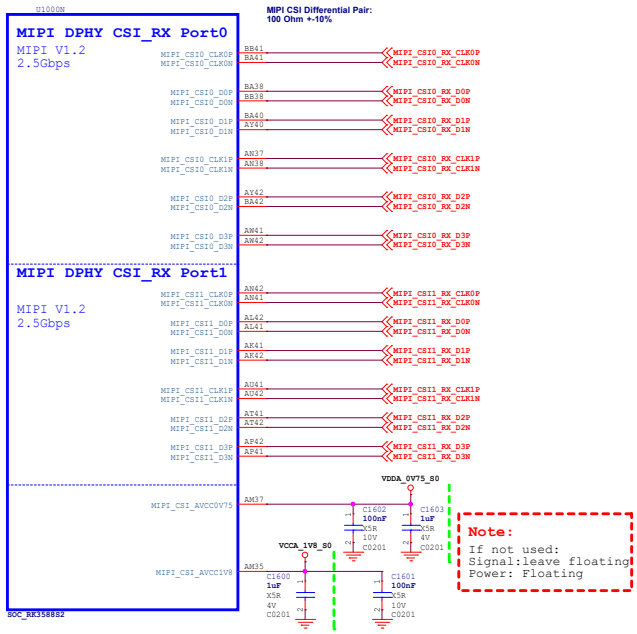




Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	15.RK3588S2_SARADC/1.8V GPIO				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	15 of 53

RK3588S2(MIPI_DPHY CSI RX)



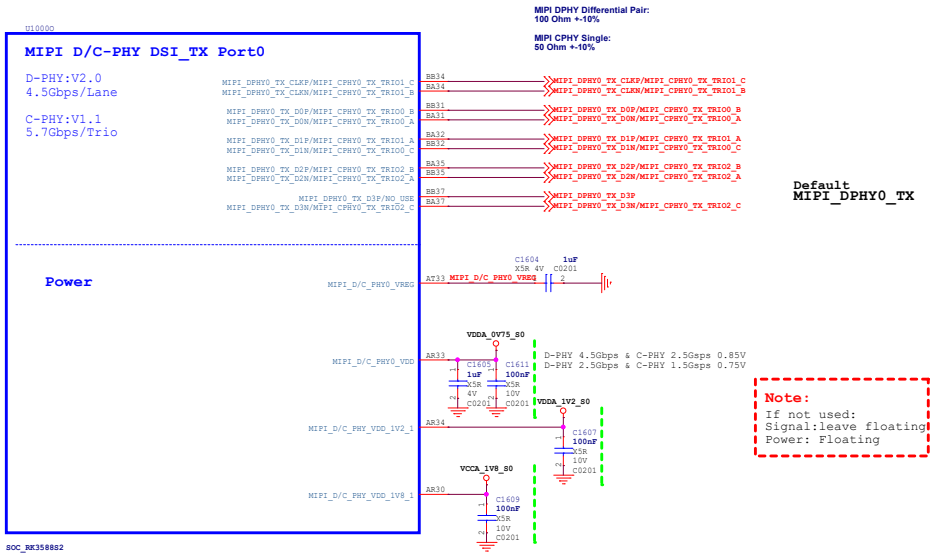
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

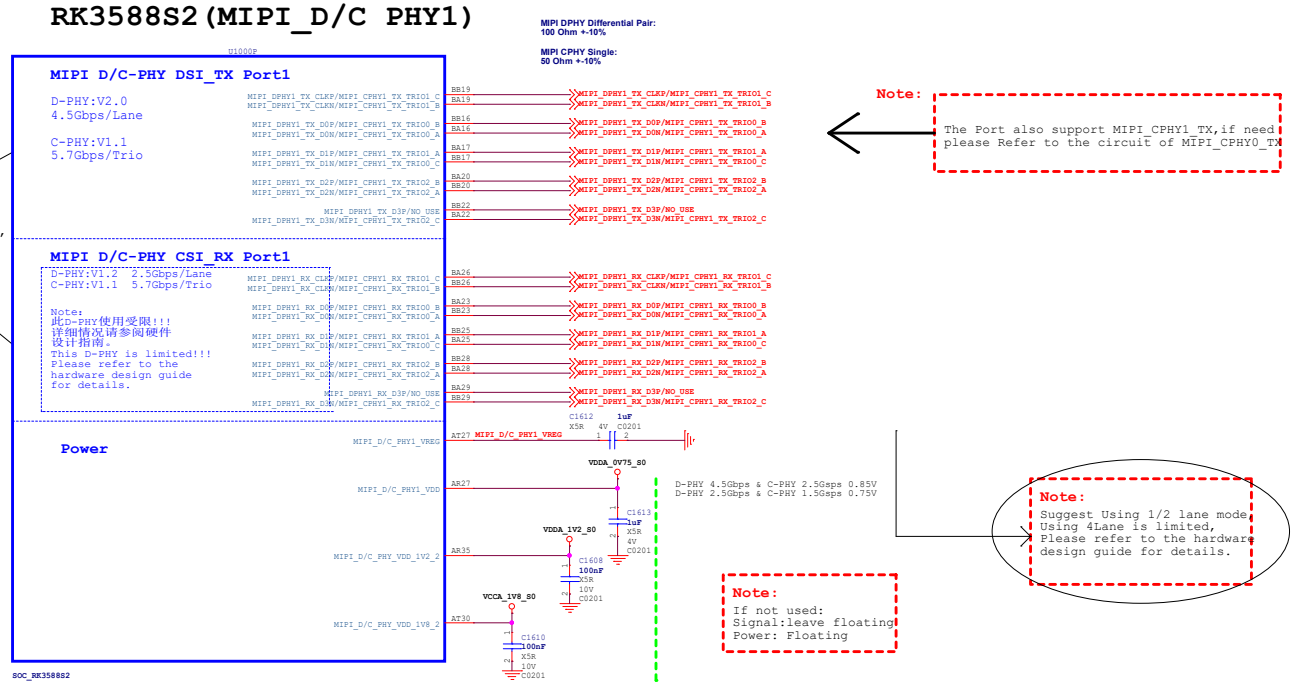
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S2(MIPI_D/C PHY0)



Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S2(MIPI_D/C PHY1)



TX and RX port must work in the same mode, DPHY or CPHY

Note:
The Port also support MIPI_CPHY1_TX,if need please Refer to the circuit of MIPI_CPHY0_TX

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

Note:
If not used:
Signal:leave floating
Power: Floating

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S2_Tablet_REF
File:	16.RK3588S2_MIPI Interface
Date:	Monday, October 13, 2025
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	16 of 53

RK3588S2(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

eDP TX
100 Ohm ±10%

U1000Q

HDMI TX/eDP1.3 MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_D0P/EDP_TX0_D0P	BB4	EDP_TX0_D0P/HDMI0_TX0P
HDMI_TX0_D0N/EDP_TX0_D0N	BA4	EDP_TX0_D0N/HDMI0_TX0N
HDMI_TX0_D1P/EDP_TX0_D1P	BA5	EDP_TX0_D1P/HDMI0_TX1P
HDMI_TX0_D1N/EDP_TX0_D1N	BB5	EDP_TX0_D1N/HDMI0_TX1N
HDMI_TX0_D2P/EDP_TX0_D2P	BB7	EDP_TX0_D2P/HDMI0_TX2P
HDMI_TX0_D2N/EDP_TX0_D2N	BA7	EDP_TX0_D2N/HDMI0_TX2N
HDMI_TX0_D3P/EDP_TX0_D3P	BA2	EDP_TX0_D3P/HDMI0_TX3P
HDMI_TX0_D3N/EDP_TX0_D3N	BB2	EDP_TX0_D3N/HDMI0_TX3N
HDMI_TX0_SBDP/EDP_TX0_AUXP	BA1	EDP_TX0_AUXP/HDMI0_TX_SBDP
HDMI_TX0_SBDN/EDP_TX0_AUXN	AY1	EDP_TX0_AUXN/HDMI0_TX_SBDN

HDMI/eDP_TX0_REXT — AY3 — HDMI/eDP_TX0_REXT — R1708 1 — 2 8.2K 1% R0201 — HDMI_VDDA0V85_S0

POWER

HDMI/EDP_TX0_VDD_0V75_1	AM13	C1710 100nF X5R 10V C0201; C1711 4.7uF X5R 6.3V C0402; C1718 Actual Setting 0.8375V 10uF X5R 6.3V C0603
HDMI/EDP_TX0_VDD_0V75_2	AN12	
HDMI/EDP_TX0_AVDD_0V75	AN10	C1712 100nF X5R 10V C0201; C1725 1uF X5R 4V C0201
HDMI/EDP_TX0_VDD_IO_1V8	AK12	C1713 100nF X5R 10V C0201; C1714 4.7uF X5R 6.3V C0402; C1716 4.7uF X5R 6.3V C0402
HDMI/EDP_TX0_VDD_CMN_1V8	AL14	

VCCA_1V8_S0

SOC_RK3588S2

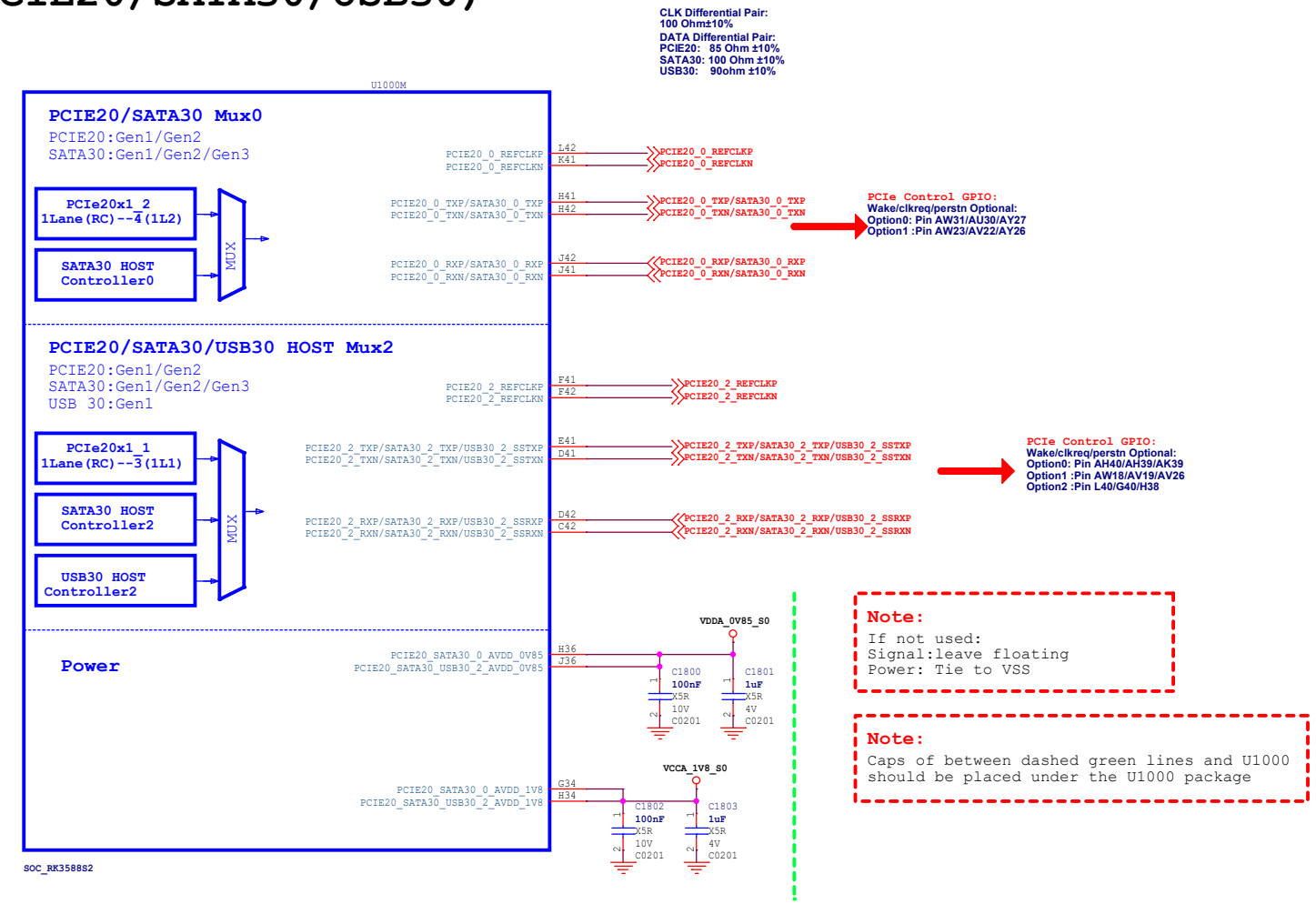
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	17.RK3588S2_HDMI/eDP Interface				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	17 of 53

RK3588S2(PCIE20/SATA30/USB30)

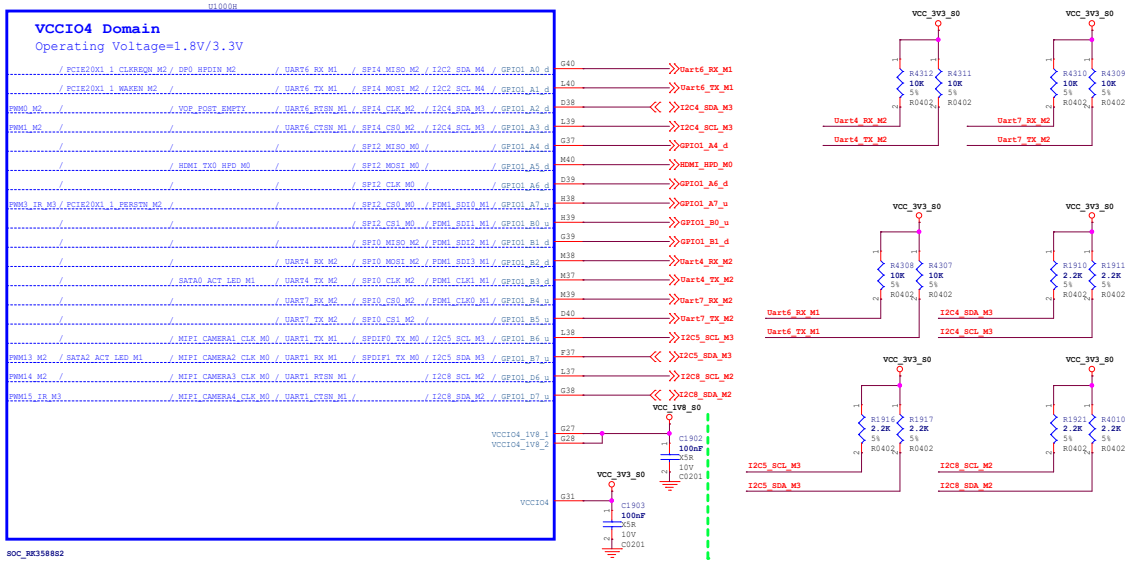


PCIe2.0 PHY

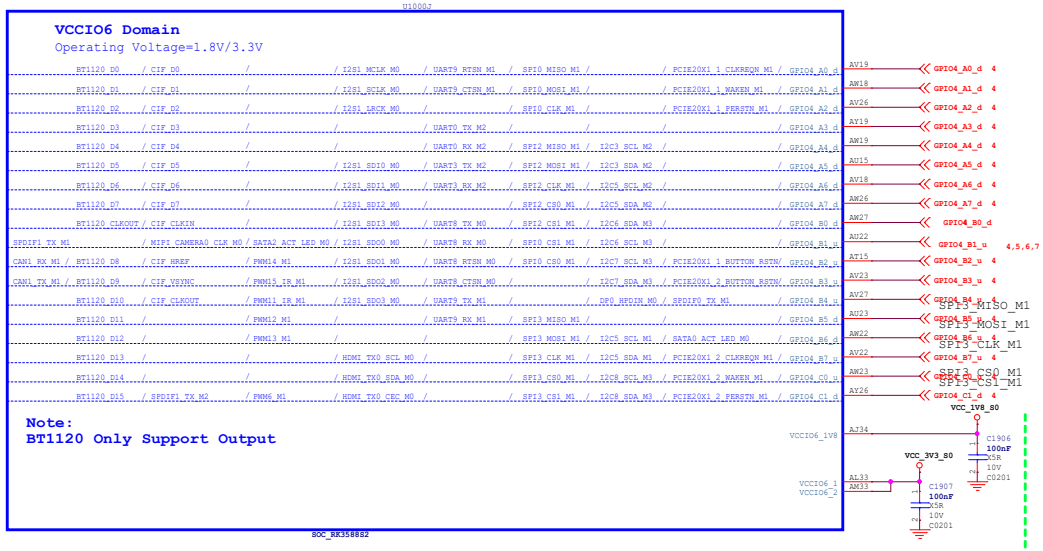
Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	18.RK3588S PCIE2/SATA3/USB3 PHY				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	18 of 53

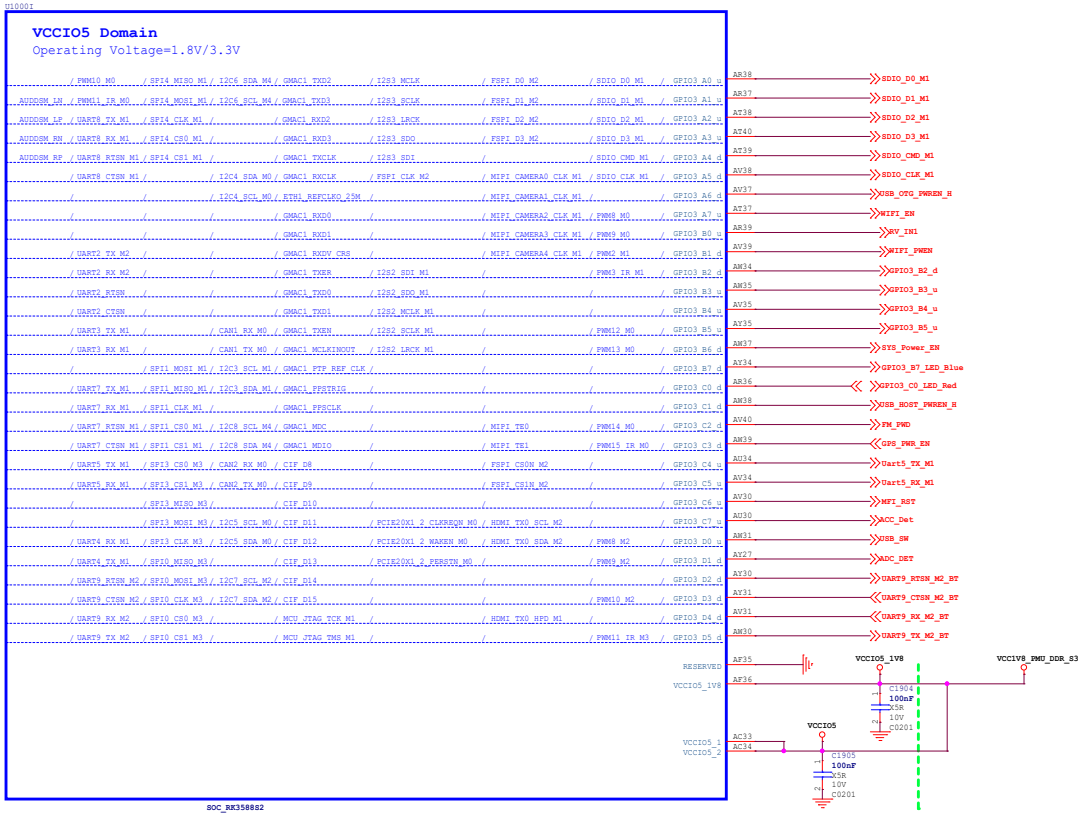
RK3588S2 (VCCIO4 Domain)



RK3588S2 (VCCIO6 Domain)



RK3588S2 (VCCIO5 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588S2_Tablet_REF		
File:	19.RK3588S2 1.8V/3.3V GPIO		
Date:	Monday, October 13, 2025	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet:	19 of 53

PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1
PMIC_PWR_CTRL2
PMIC_INT_L
PWRON_L
PMIC_RESET_L
PMIC_EXT_EN_OUT
PMIC_SPI_CLK
PMIC_SPI_CS
PMIC_SPI_MOSI

VCC_SYSIN
D2200 AZ5825-01F ESD0402

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

PMIC RK806-1 BUCK

U2200A

Default:0.85V
Low frequency:
0.85V-->0.75V

VDD_DDR_S0 — Feedback from RK3588S2

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

VDDQ_DDR_S0

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

VCC_3V3_S3

VCC1V8_PMU_DDR_S3 — R2210 0R/NC 5% DNP R0603

VCC_1V8_S3_PLDO6 — Default:1.8V — R2211 0R R0603 5%

BUCK5 2.5A	VCC5	SW5
BUCK1 6.5A	VCC1_1 VCC1_2	SW1_1 SW1_2
BUCK6 2.5A	VCC6	SW6
BUCK2 5A	VCC2_1 VCC2_2	SW2_1 SW2_2
BUCK9 2.5A	VCC9	SW9
BUCK3 5A	VCC3	SW3
BUCK8 2.5A	VCC8	SW8
BUCK4 5A	VCC4	SW4
BUCK10 2.5A	VCC10	SW10
BUCK7 2.5A	VCC7	SW7

VDD_GPU_S0 — Feedback from RK3588S2
VDD_CPU_LIT_S0 — Feedback from RK3588S2
VDD_LOGIC_S0 — Feedback from RK3588S2
VDD_VDENC_S0 — Feedback from RK3588S2

RK806-1

PMIC RK806-1 Managerment

U2200C

VCCIO: (IIC/SPI)CS, (SDA)MOSI, (SCL)CLK, (PWRCTRL3)SO, PWRCTRL2, PWRCTRL1, (M/S)EXT_EN, INT, RESETB, ePAD
VCCA: SYNC_CLK, SYNC, VDC, PWRON

PMIC_SPI_CS, PMIC_SPI_MOSI, PMIC_SPI_CLK, PMIC_PWR_CTRL2, SLEEP1_RESET1_DEVOFF1_VSEL1, PMIC_EXT_EN_OUT, PMIC_INT_L, PMIC_RESET_L

PMIC_VDC — D2600 BZT52C3V0 SOD_123 — PWRON_L

RK806-1

RK3588S2 nPOR
TSADC_SHUT
RK806-1 RESETB
Reset Key

Note:

- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

PLDO	0.5A	PLDO1	VCCA_1V8_S0 — Default:1.8V
	0.3A	PLDO2	VCC_1V8_S0 — Default:1.8V
	0.3A	PLDO3	VDDA_1V2_S0 — Default:1.2V
	0.5A	PLDO4	VCCA_3V3_S0 — Default:3.3V
	0.3A	PLDO5	VCCIO_SD_S0 — Default:3.3V
NLDO	0.3A	NLDO1	VDD_0V75_S3 — Default:0.75V
	0.3A	NLDO2	VDDA_DDR_PLL_S0 — Default:0.85V; Low frequency:0.85V-->0.75V
	0.5A	NLDO3	VDDA_0V75_S0 — Default:0.75V
	0.5A	NLDO4	VDDA_0V85_S0 — Default:0.85V
	0.3A	NLDO5	HDMI_VDDA0V85_S0 — Default:0.75V Reserved

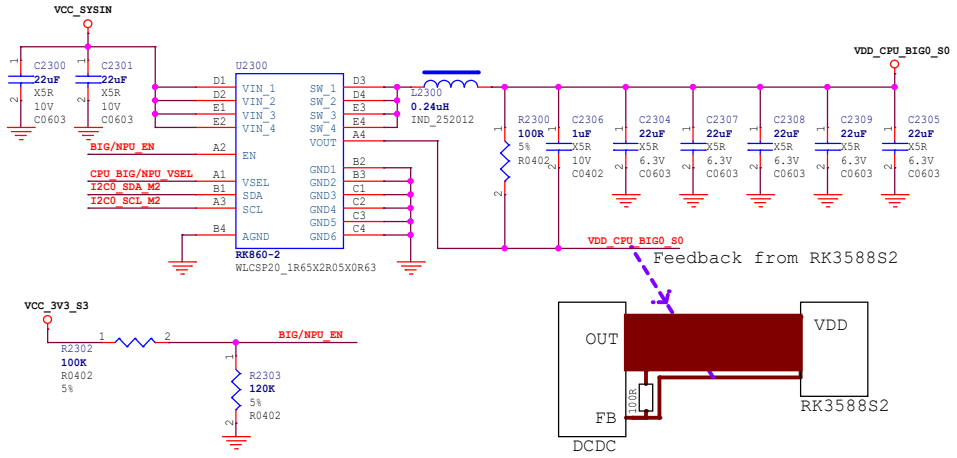
VCC_2V0_PLDO_S3 — C2247 1uF X5R 10V C0402
VCC_SYSIN — C2252 1uF X5R 10V C0402
VCC_1V1_NLDO_S3 — C2257 1uF X5R 10V C0402
VCC_1V1_NLDO_S3 — C2264 1uF X5R 10V C0402

VCCA_1V8_S0 — R2274 0R 5% R0402 — AVDD1V8_DDR_PLL_S0 — C2290 1uF X5R 10V C0402

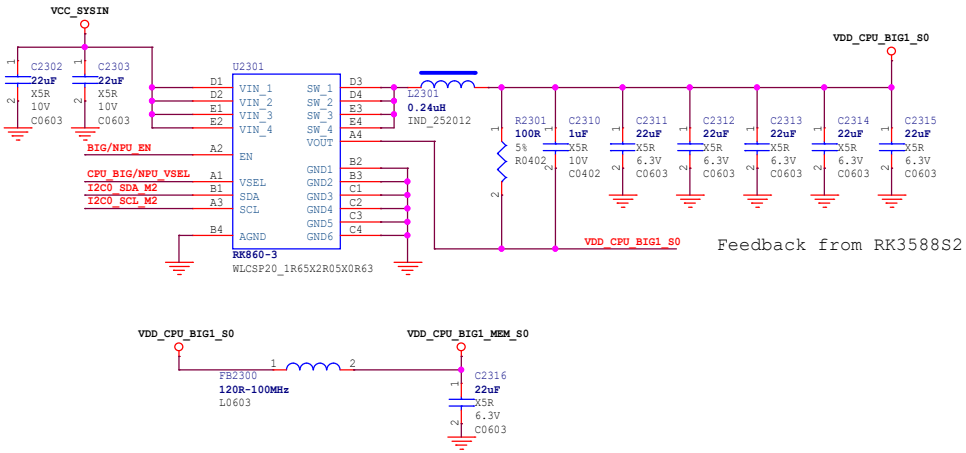
RK806-1

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588S2_Tablet_REF
File:	22.Power-PMIC_RK806-1
Date:	Monday, October 13, 2025
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	22 of 53

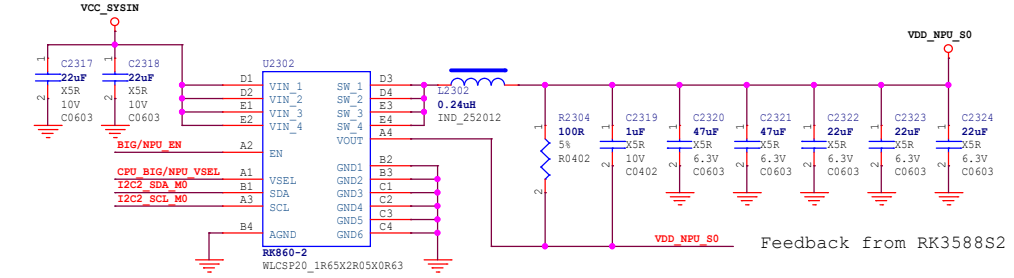
VDD_CPU_BIG0



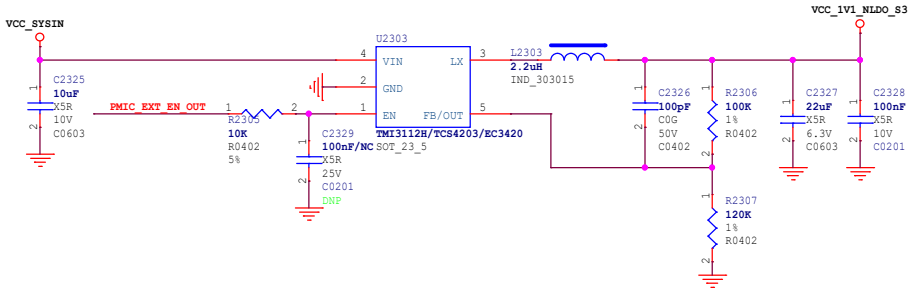
VDD_CPU_BIG1



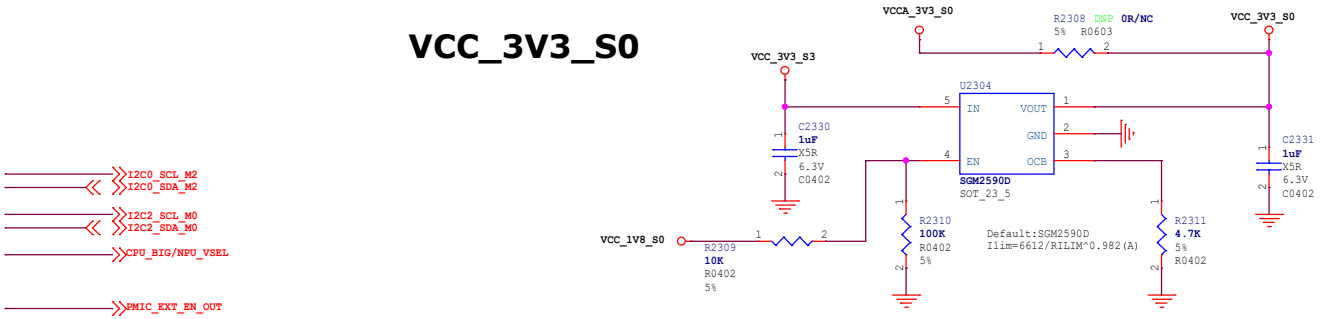
VDD_NPU



VCC_1V1_NLDO



VCC_3V3_S0

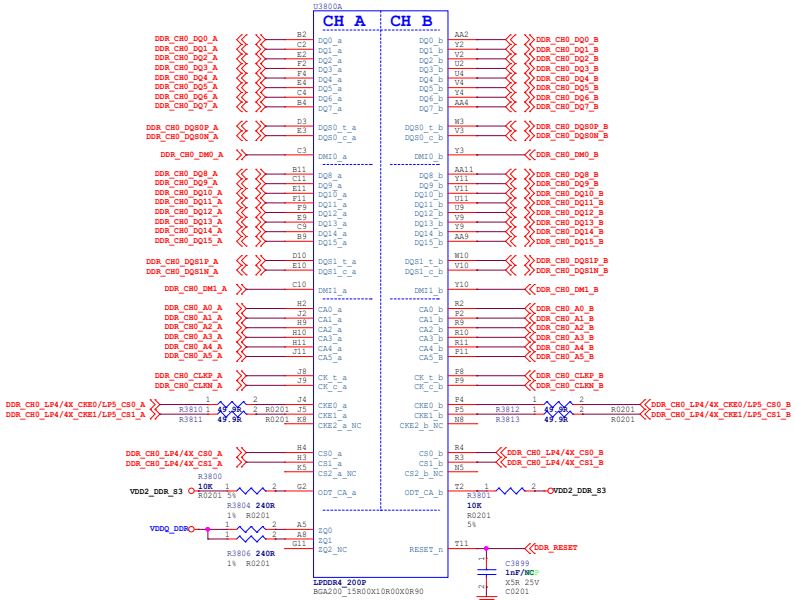


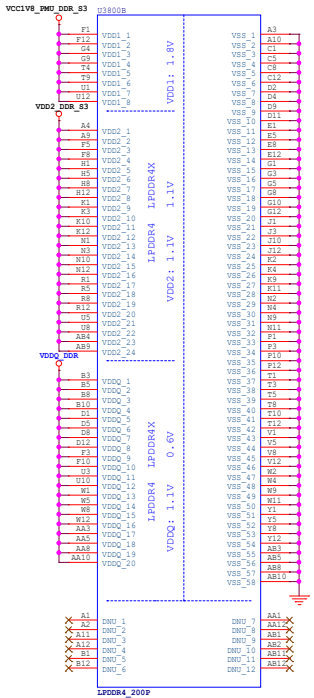
Load Switch

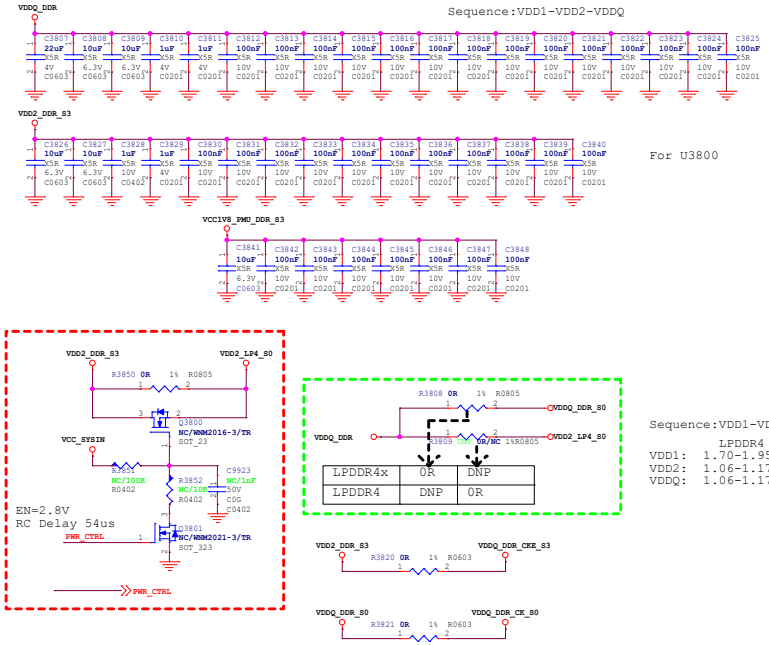
Load Switch should Select a discharge resistor with a discharge resistance less than 50ohm

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S2_Tablet_REF				
File:	23.Power_Ext Discrete				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	23 of 53

DRAM-LPDDR4/4x_2X32bit

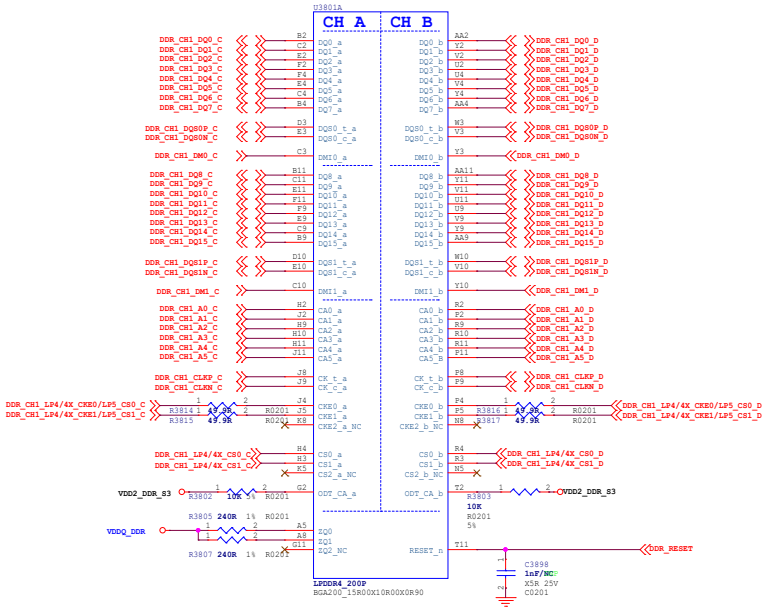


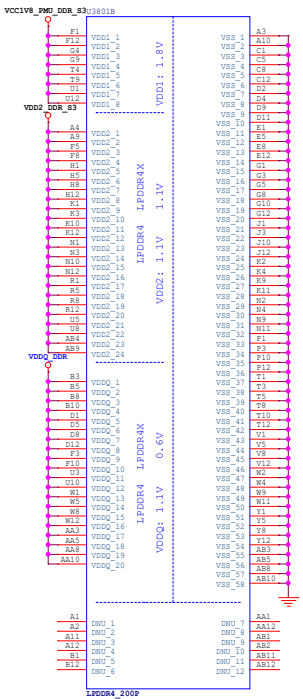


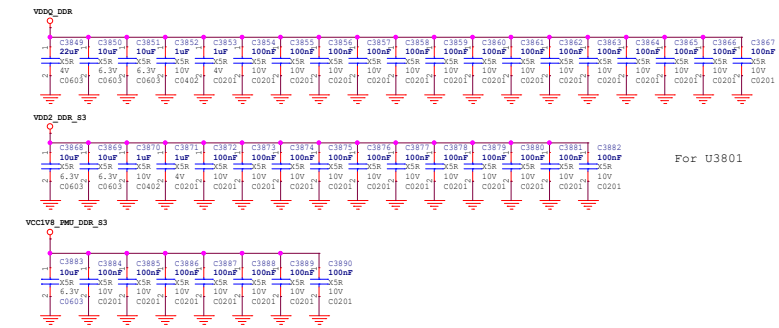


	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

LPDDR4x	0R	DNP
LPDDR4	DNP	0R





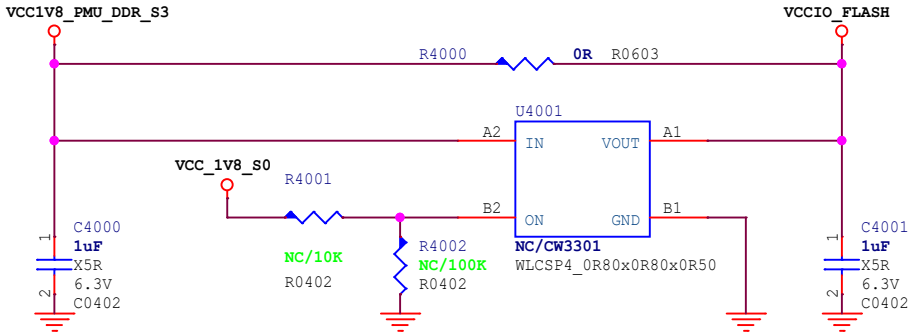


Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588S2_Tablet_REF		
File:	38.DRAM-LPDDR4/4X_200P_2X32bit		
Date:	Monday, October 13, 2025	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet:	26 of 53

Flash Power

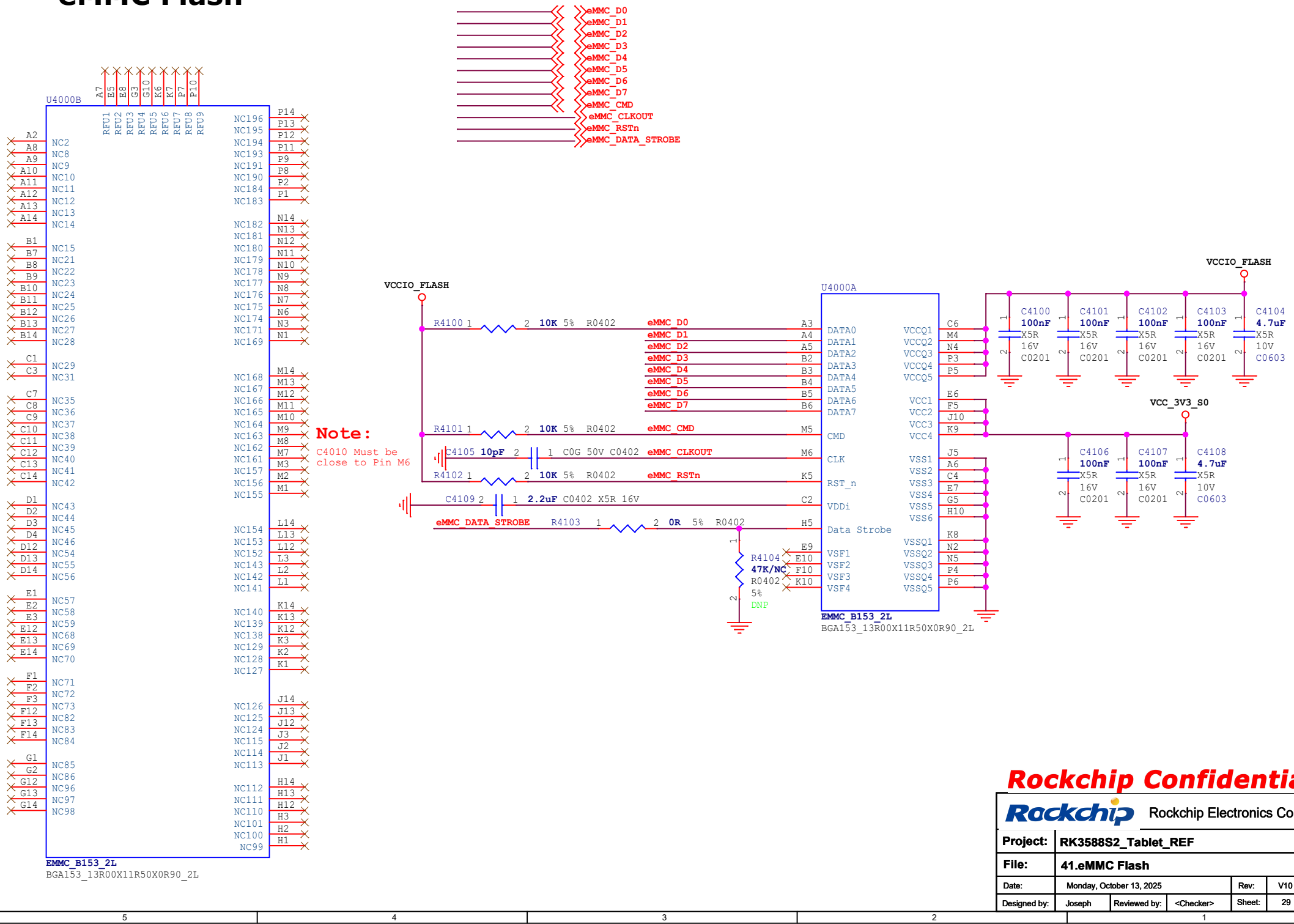
PWR_CTRL



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	40.Flash Power				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	28 of 53

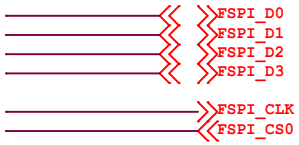
eMMC Flash

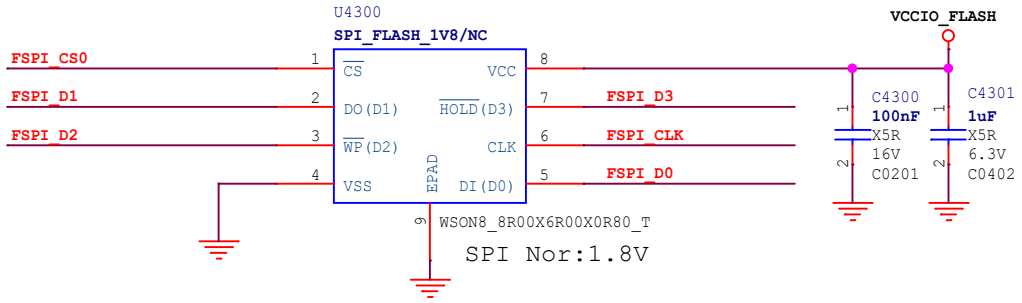


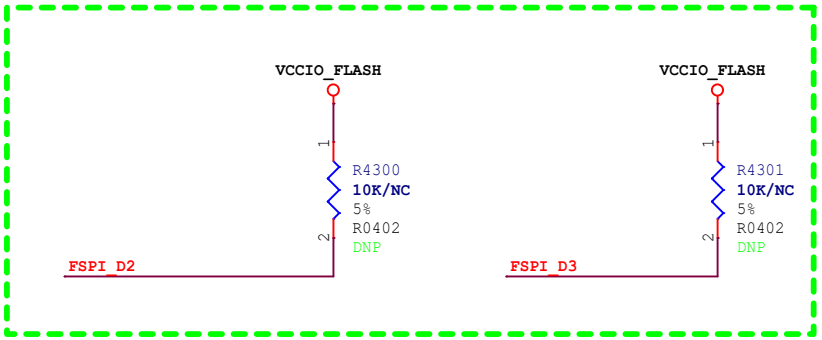
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	41.eMMC Flash				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	29 of 53

SPI FLASH



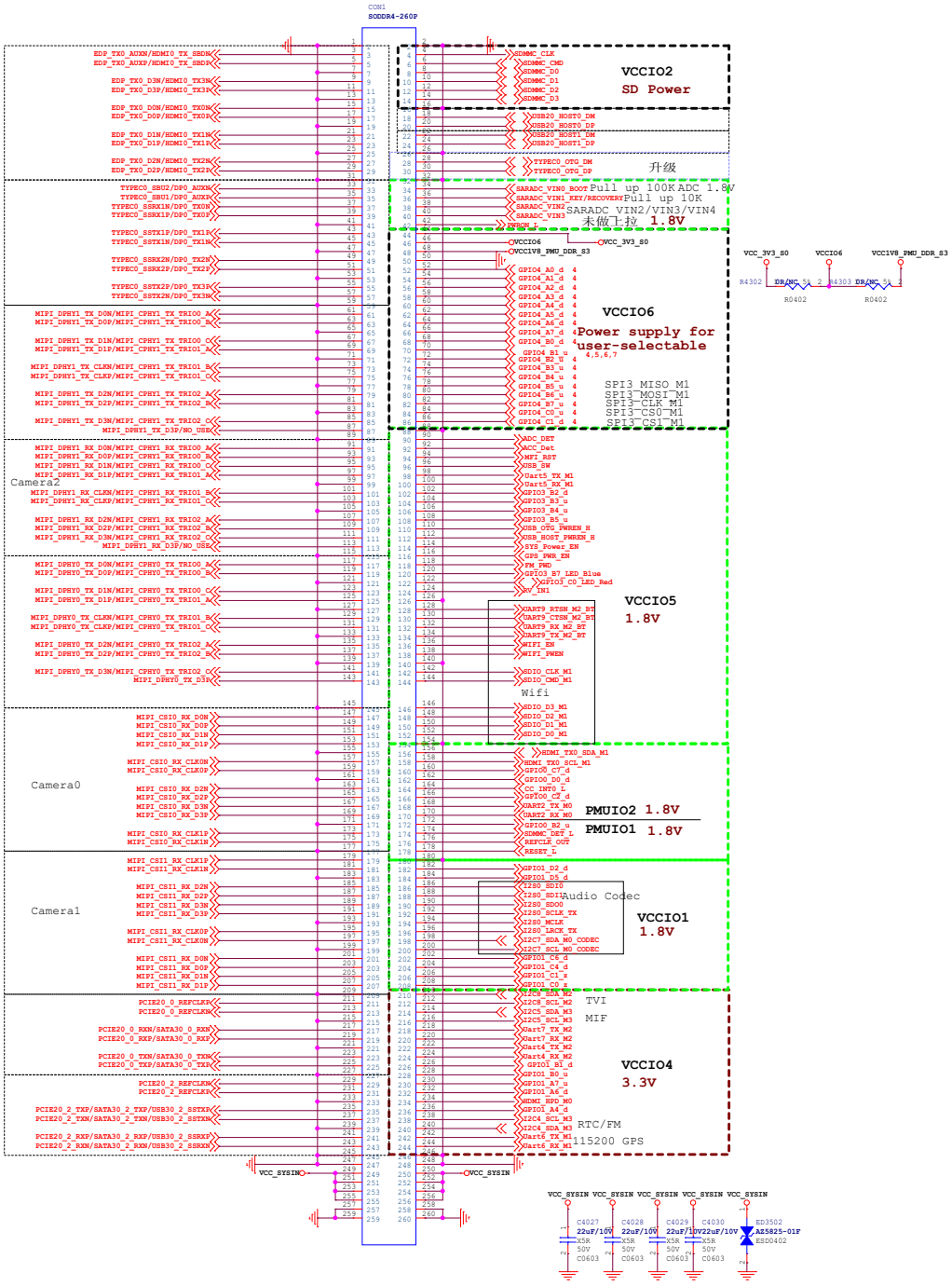




Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

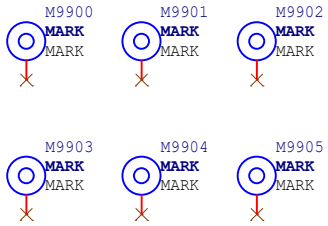
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588S2_Tablet_REF				
File:	43.Flash-SPI FLASH(opt)				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	31 of 53

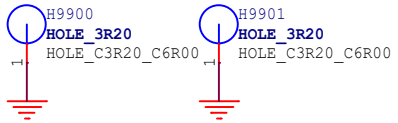


Project:	RK3588S2_Tablet_REF		
File:	44.SODM CONNECTOR		
Date:	Monday, October 13, 2025	Rev:	V0.9
Designed by:	Wang	Sheet:	44 of 44

PCB Mark Point

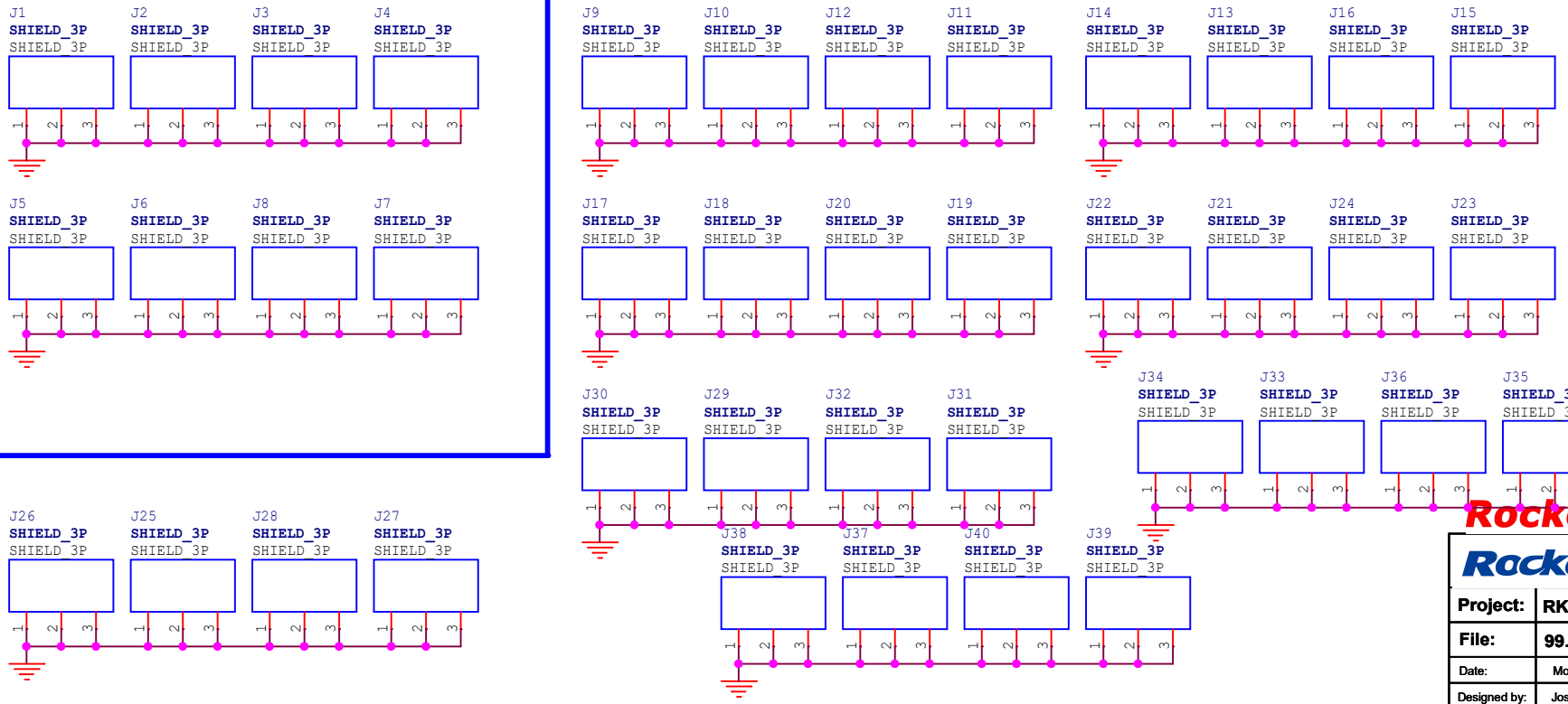


Mechanical Hole



Heatsink

Shield



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588S2_Tablet_REF				
File:	99.Mark/Heatsink				
Date:	Monday, October 13, 2025			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	53 of 53