REF Schematic for RK3568

Main Functions Introduction

1)PMIC: RK809-5+DiscretePower
2)RAM: DDR4 2x16Bit------------------Default
 Option:LPDDR4/4x 1X32bit(200ball)
 Option:DDR3 4x16bit
 Option:DDR3 4x16bit+2x16bit ECC
 Option:DDR4 2x16bit+1x16bit ECC
 Option:LPDDR3 1x32bit(178ball)
 Option:DDR4 4x16bit
3)ROM: eMMC--------------------------Default
 Option:Nand Flash
 Option:SPI Flash
4)Support:1 x Micro SD Card3.0
5)Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1   + 1 x SATA3.0 Port2 ----------Default
   Option:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1   + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1   + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
   Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1   + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
   Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
6)Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3 -- ------Default
7)Support:4G module Via MiniPCIe2.0 Slot With PCIE2.0 and USB2.0 HOST3 function ------Option
8)Support:2 x 1Lane PCIe3.0 Connector (RC Mode) ------Default
   Option:1 x 2Lanes PCIe3.0 Connector (RC Mode)
   Option:1 x 2Lanes PCIe3.0 Connector (EP Mode)
9)Support:1 x HDMI2.0 TX
10)Support:1 x LCM MIPI DSI TX0 ----------Default
   Option:1 x LCM MIPI DSI TX1
   Option:1 x LCM LVDS TX
   Option:1 x LCM Dual MIPI DSI TX
   Option:1 x LCM eDP TX
11)Support:1 x VGA OUT ----------Default
12)Support:1 x 4Lanes Camera MIPI CSI RX ----------Default
   Option:2 x 2Lanes Camera MIPI CSI RX
   Option:1 x HDMI1.4 RX(HDMI to MIPI CSI)
13)Support:a/b/g/n/ac 2X2 SDIO WIFI5+BT5.0+PCM --------Default
   Option:a/b/g/n/ac 1X1 SDIO WIFI+BT+PCM
   Option:a/b/g/n/ac/ax 2X2 PCIe WIFI6+BT5.0+PCM
14)Support:1 x 10/100/1000M Ethernet(RGMII1_M1) -------Default
   Option:1 x 10/100/1000M Ethernet(RGMII0) or 1 x 10/100M Ethernet(RMII0)
   Option:1 x 10/100/1000M PCIe Ethernet Card or 2 x 10/100/1000 Ethernet(QSGMII) or 1 x 10/100/1000 Ethernet(SGMII)
15)Support:1 x Headphone output ----------Default
16)Support:1 x ECM MIC + 1 x Speaker out ----------Default
   Option:4 x MEMS MIC + 1 x Speaker out + Loopback or 2 x MEMS MIC + 1 x Speaker out + Loopback
   Option:4 x MEMS MIC + 2 x Speaker out + Loopback
17)Support:1 x IR Receiver ----------Default
18)Support:Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
19)Support:3 x UART + 1 x RS485 + 1 x CAN FD(Option)
20)Support:Debug UART and ARM JTAG

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Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02-04	Zhangdz	1:Revision preliminary version	
V1.1	2021-06-11	Zhangdz	1:Change content Please Refer to: RK3568_AIoT_REF_SCH_V11_20210611_Modify_Notes	
V1.1	2024-03-05		20页：R2020 改为49.9K 5V 改成3.3V 36页：R3609 R3617 R6978 R6973 R6961 R6956 R6996 R6990 改成10K 删除R3611 R3614 R6972 R6971 R6955 R6953 R6989 R6987 0R电阻 删除D3710 D3600 D3709 D3711 增加LS1 LS2 LS3 LS4 增加CS1 CS2 CS3 CS4 CS5 CS6 CS7 CS8 增加DS1 DS2 DS3 DS4 增加F1 F2 F3 F4 F5 F6 F7 F8 增加 JS1 JS2 BOM 相应增加2.54MM两个跳帽 删除：ED3603 ED3602 ED3711 ED3710 ED3709 ED3708 ED3713 ED3712 删除：D3602 L2000改成L4040封装 4.7UH 增加：RS1 RS2 RS3 RS4 RS5 RS6 RS7 RS8 10K R0402 增加US1 US2 GT4946BEY SOP8 增加PC1 PC2 PC3 PC4 EL817S1 增加：DS5 DS6 DS7 DS8 DS9 DS10 DS11 DS12 增加：RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8 RD9 RD10 RD11 RD12 RD13 RD14 RD15 RD16 增加：QS1 QS2 QS3 QS4 三极管3904 SOT23 增加：R10008 0R 删除：R3649 R3650 R3646 R3647 删除：ZD2001 ZD2002 ZD2003 ZD2004 预留U9506 这一路电源不上件 接显示屏或者摄像头时候上	

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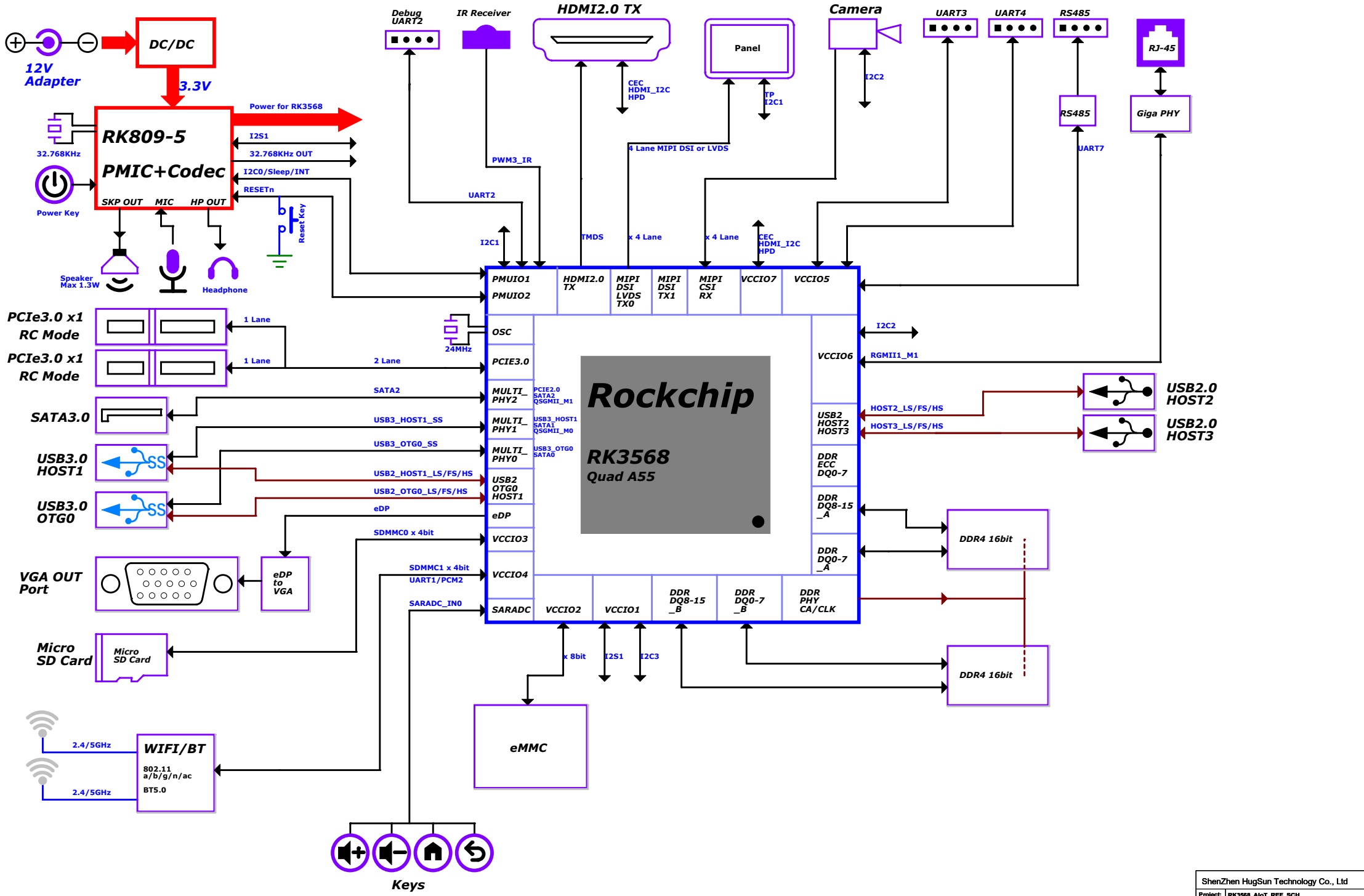
RK3568 Ref Block Diagram(Default configuration)



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Default Power Diagram

12V Adapter

DC/DC 3000mA Seq:0 Max:

VCC3V3_SYS

RK809-5

Power on Sequence

VCC1	BUCK1 0.5V~2.4V, 2.5A max	Seq:1	VDD_LOGIC Max:	RK3568_Logic	
VCC2	BUCK2 0.5V~2.4V, 2.5A max	Seq:2	VDD_GPU Max:	RK3568_GPU	
VCC3	BUCK3 0.5V~2.4V, 1.5A max	Seq:3	VCC_DDR Max:	RK3568_DDRC DRAM	
VCC4	BUCK4 0.5V~3.4V, 1.5A max	OFF	VDD_NPU Max:	RK3568_NPU	
	LDO1 0.6V~3.4V, 400mA max	OFF	VDDA0V9_IMAGE Max:	MIPI_CSI_RX_AVDD_0V9 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_0V9 Max: MIPI_DSI_TX1_AVDD_0V9 Max: EDP_TX_AVDD_0V9 Max: HDMI_TX_AVDD_0V9 Max:	
VCC5	LDO2 0.6V~3.4V, 400mA max	Seq:1	VDDA_0V9 Max:	SYSPLL_AVDD_0V9 Max: USB2_AVDD_0V9 Max: USB3_AVDD_0V9 Max: MULTI_PHY_AVDD_0V9 Max: PCIE30_AVDD_0V9 Max:	
	LDO3 0.6V~3.4V, 100mA max	Seq:1	VDDA0V9_PMU Max:	PMU_VDD_LOGIC_0V9 Max: PMUPLL_AVDD_0V9 Max:	
	LDO4(Codec VDDIO) 0.6V~3.4V, 400mA max	OFF	VCCIO_ACODEC Max:	VCCIO1--I2S1/PDM MIC/PDM ADC	
VCC6	LDO5 0.6V~3.4V, 400mA max	Seq:4	VCCIO_SD Max:	VCCIO3--SDMMC0	
	LDO6 0.6V~3.4V, 400mA max	Seq:2	VCC3V3_PMU Max:	PMUIO1/ PMUIO2	
	LDO7 0.6V~3.4V, 400mA max	Seq:2	VCCA_1V8 Max:	SYSPLL_AVDD_1V8 Max: USB2_AVDD_1V8 Max: USB3_AVDD_1V8 Max: MULTI_PHY_AVDD_1V8 Max: PCIE30_AVDD_1V8 Max: SARADC_AVDD_1V8 Max:	
VCC7	LDO8 0.6V~3.4V, 400mA max	Seq:2	VCCA1V8_PMU Max:	PMUPLL_AVDD_1V8 VCC1V8_DDR	
	LDO9 0.6V~3.4V, 400mA max	OFF	VCCA1V8_IMAGE Max:	MIPI_CSI_RX_AVDD_1V8 Max: MIPI_DSI_TX0/LVDS_TX0_AVDD_1V8 Max: MIPI_DSI_TX1_AVDD_1V8 Max: EDP_TX_AVDD_1V8 Max: HDMI_TX_AVDD_1V8 Max: VCC18_LCD(Option) Max:	
VCC8	Switch2 2.1 A max, Rdson=100mΩ	Seq:4	VCC3V3_SD Max:	Micro SD Card	
	Switch1 2.1 A max, Rdson=90mΩ	Seq:4	VCC_3V3 Max:	USB3_AVDD_3V3 Max: USB2_AVDD_3V3 Max: VCCIO5,VCCIO7 Max: eMMC_VCC / Nand_VCC Max: VCC3V3_PHY0/1/2 Max: VCC3V3_TP Max: IR Receiver Max: UART Device Max: RS485 Device Max: CAN IC Max:	
VCC9	BUCK5: 1.5V~3.6V, 2.5 A max	Seq:2	VCC_1V8 Max:	OTP_VCC18 Max: VCCIO2(Default) --eMMC/Nand IO Max: VCCIO4(Default) Max: VCCIO6(Default) Max: GiGa PHY0/1 IO-Option Max: WIFI/BT IO Max:	
VCC_RTC					

VCC5V0_SYS

EXT DC/DC ,5A Seq:2A — VDD_CPU Max: — RK3568_CPU

EXT LDO ,0.3A Seq:2A — VCC2V5_DDR Max: — DDR4 DRAM

VCC3V3_SYS

- Mos-->LCD Panel Max:
- Mos-->VCC3V3_VGA Max:
- Mos-->RK628D Max:
- WIFI/BT VBAT Max:
- LDO-->Camera 1.2V Max:
- LDO-->Camera 1.8V Max:
- RTC IC Max:

MOS OFF
- PCIe Slot Max:
- SATA Max:

DC/DC 3000mA Seq:0 — VCC5V0_USB Max:
- SATA Max:
- USB HOST Max:

DC/DC 3000mA Seq:0 — VCC5V0_SYS Max:
- RK809_SPK_PA Max:
- MOS → VCC5V0_VGA Max:
- LDO → VCC3V3_PI6C Max:
- LDO → Camera 2.8V Max:
- DDR VTT Max:
- LCM Backlight Max:
- MOS → VCC5V_HDMI_TX Max:
  - CAN transceiver IC Max:
  - EXT SPK PA Max:
- EXT DC/DC → VCC1V05_QS_VDDL Max:
- EXT DC/DC → VCC3V3_QS_VDDH Max:

DC/DC 3000mA — VCC3V3_PCIE Max:

DC/DC 3000mA — VCC3V3_MINIPCIE Max:

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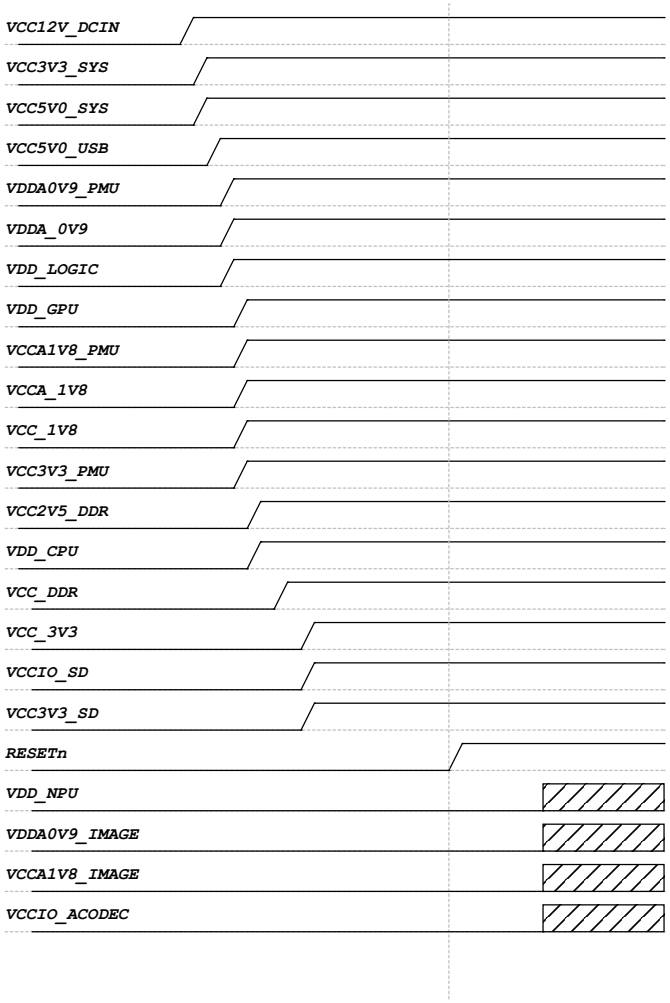
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

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IO Power Domain Map

If IO domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

IO Domain	Pin Num	Support IO Voltage		Notes	Default IO Domain Voltage		
		3.3V	1.8V		Supply Power Net Name	Power Source	Voltage
PMUIO0 (PMUPLL_AVDD_1V8)	Pin Y21	✗	✓	PMUIO0 are fixed 1.8V level mode, which cannot be configured.	VCCA1V8_PMU	VCCA1V8_PMU	1.8V
PMUIO1	Pin Y20	✓	✗	PMUIO1 are fixed 3.3V level mode, which cannot be configured.	VCC3V3_PMU	VCC3V3_PMU	3.3V
PMUIO2	Pin W19	✓	✓	PMUIO2 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC3V3_PMU	VCC3V3_PMU	3.3V
VCCIO1	Pin H17	✓	✓	VCCIO1 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO_ACODEC	VCCIO_ACODEC	3.3V
VCCIO2	Pin H18	✓	✓	VCCIO2 supports 1.8V or 3.3V level mode Default is configured by hardware,namely PIN "FLASH_VOL_SEL" state determines which mode to work in.[1][2]	VCCIO_FLASH	VCC_1V8	1.8V
VCCIO3	Pin L22	✓	✓	VCCIO3 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2][3]	VCCIO_SD	VCCIO_SD	3.3V
VCCIO4	Pin J21	✓	✓	VCCIO4 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO4	VCC_1V8	1.8V
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO6	VCC_1V8	1.8V
VCCIO7	Pin V12	✓	✓	VCCIO7 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V

For example, the VCCIO4 hardware has been modified to 3.3V power supply, and the corresponding DTS must be modified to 3.3V configuration, otherwise the IO of VCCIO4 will be damaged.

If a board needs to be compatible with two voltage choices, recommended to enable BOM ID

Notes

[1]:When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

[2]:When the IO domain power supply voltage is 1.8V, the IO domain voltage configuration in DTS must be set to 1.8V mode.
If it is misconfigured to 3.3V mode, the IO function of this power domain will be abnormally;
When the IO domain power supply voltage is 3.3V, the IO domain voltage configuration in DTS must be set to 3.3V mode.
If it is misconfigured to 1.8V mode, the IO in this power domain will be in overvoltage state, and the IO will be damaged after long-term operation.

[3]:When VCCIO3 IO domain is assigned as SD card function,:
If SD3.0 mode is to be supported, VCCIO3 power supply voltage must be support configurable, 3.3V in SD2.0 mode and 1.8V in SD3.0 mode.
If only SD2.0 mode is supported (SD3.0 card only works in SD2.0 mode), VCCIO3 only needs fixed power supply of 3.3V.
When VCCIO3 IO domain is assigned as other function,:
Such as uart5 and uart6, then note [2] should be followed

Default UART Map

RK3568

UART0

UART1 — Mux — M0: UART1_M0 → BT; M1

UART2 — Mux — M0: UART2_M0 → Debug UART2 Port; M1

UART3 — Mux — M0; M1: UART3_M1 → ●●●■

UART4 — Mux — M0; M1: UART4_M1 → ●●●■

UART5 — Mux — M0; M1

UART6 — Mux — M0; M1: UART6_M1 → ●●●■

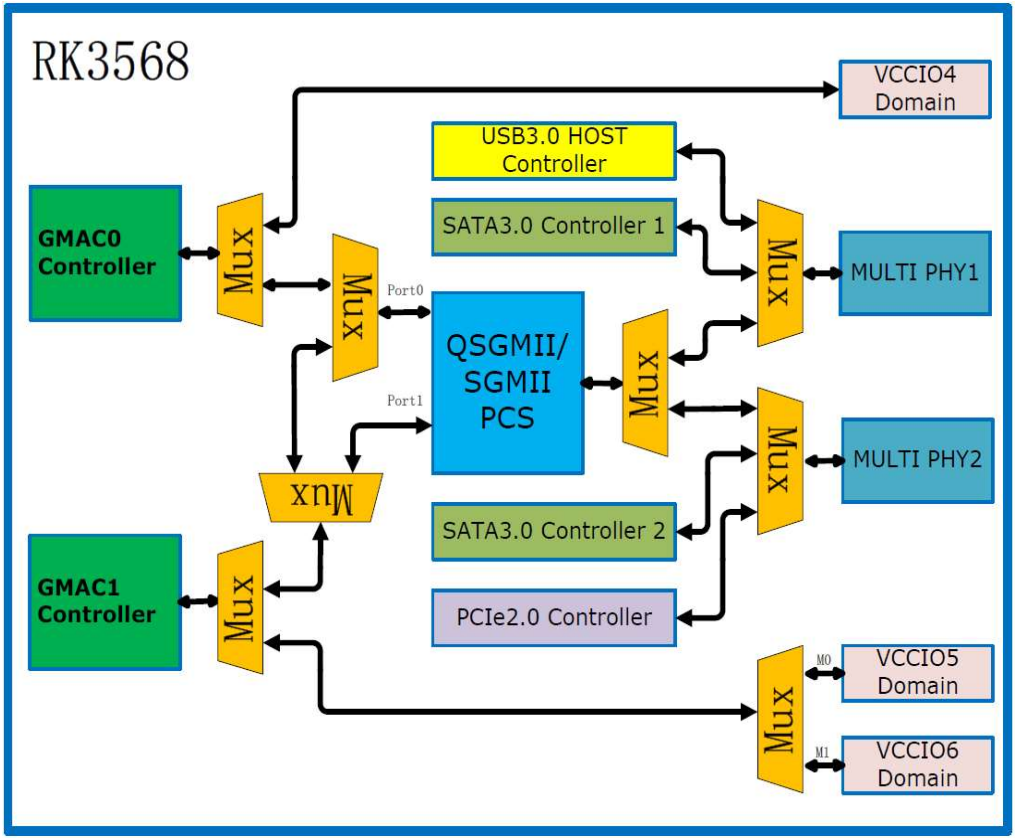
If no MicroSD Card function

UART7 — Mux — M0; M1: UART7_M1 → RS485 → RS485 → ●●●■; M2

UART8 — Mux — M0; M1

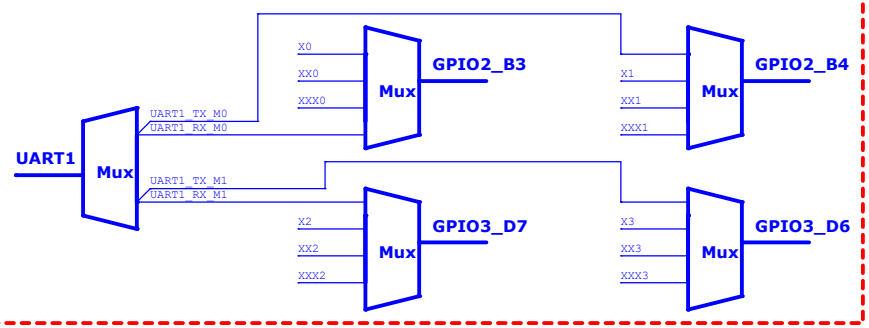
UART9 — Mux — M0; M1: UART9_M1 → ●●●■; M2

GMAC0/1 Path Map



Note:

M0 M1 M2 indicates that the same function is multiplexed to different IO
When selecting, only M0 or M1 or M2 can be selected
eg:Not supported UART1_TX_M0 and UART1_RX_M1 combination



It is suitable for other interfaces

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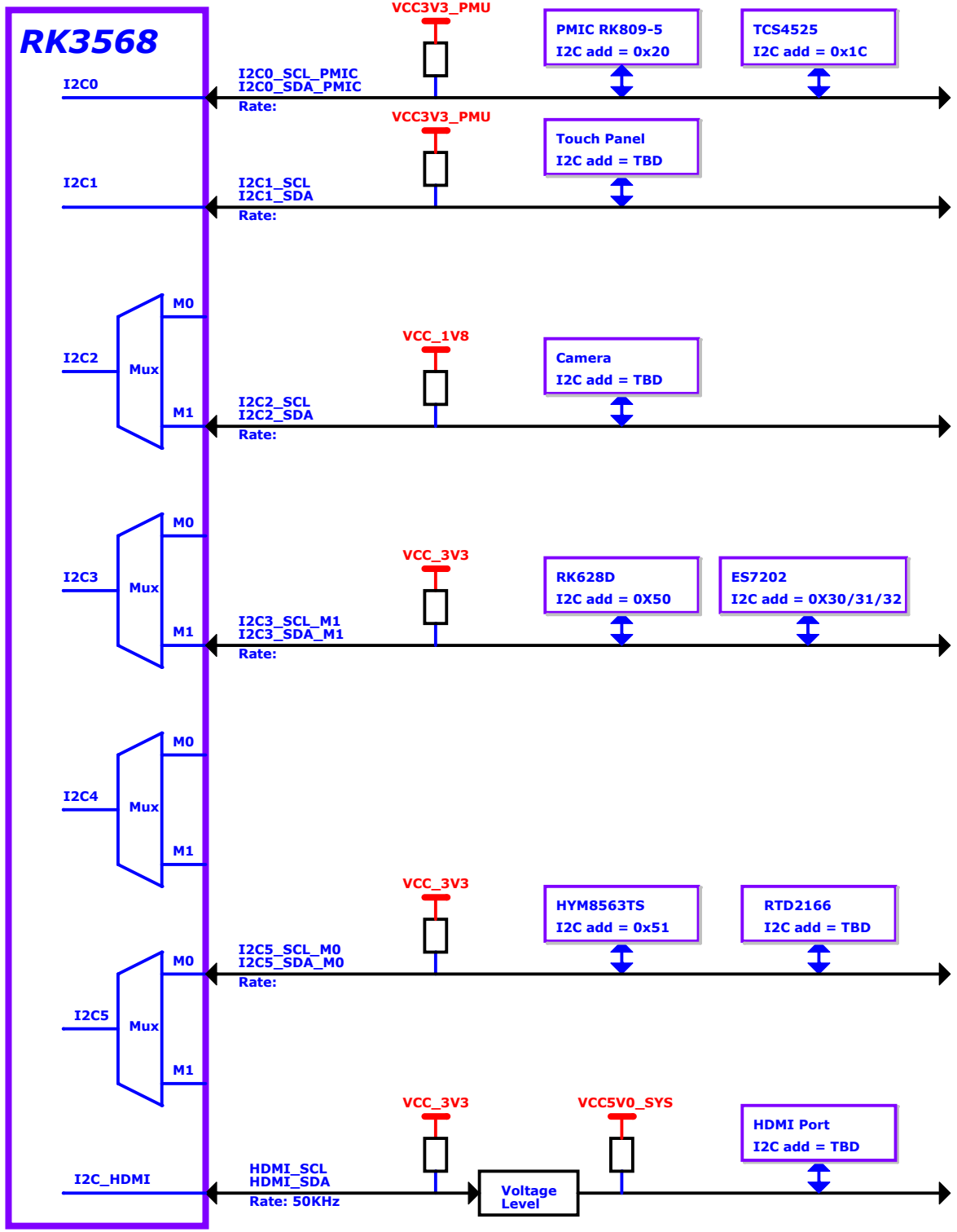
Default I2C Map

Note:
M0 M1 M2 indicates that the same function is multiplexed to different IO. When selecting, only M0 or M1 or M2 can be selected
eg:
Not supported I2C1_SCL_M0 and I2C1_SDA_M1 combination



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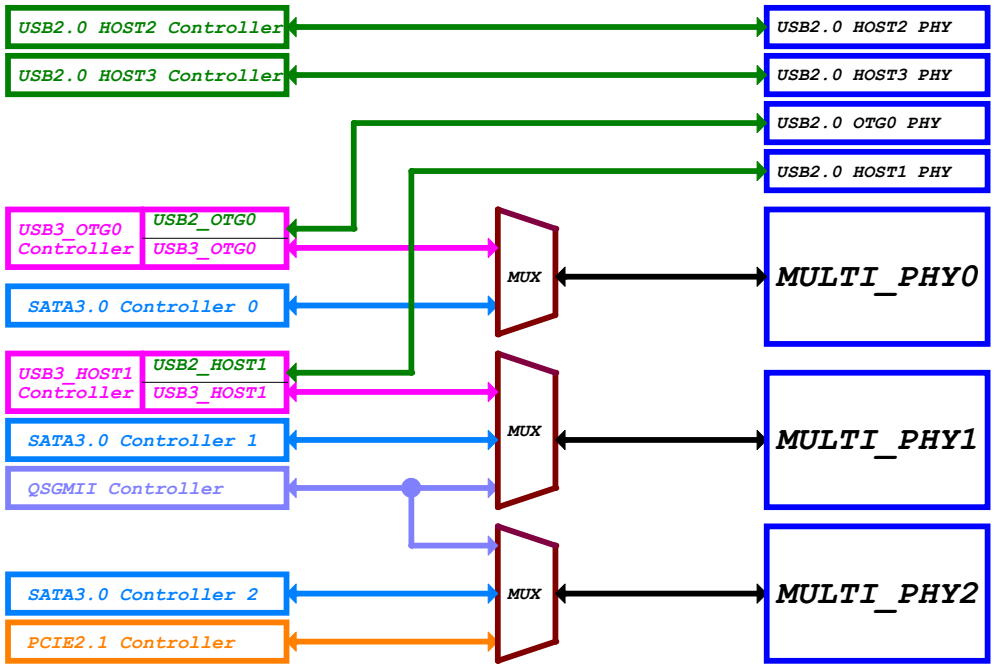
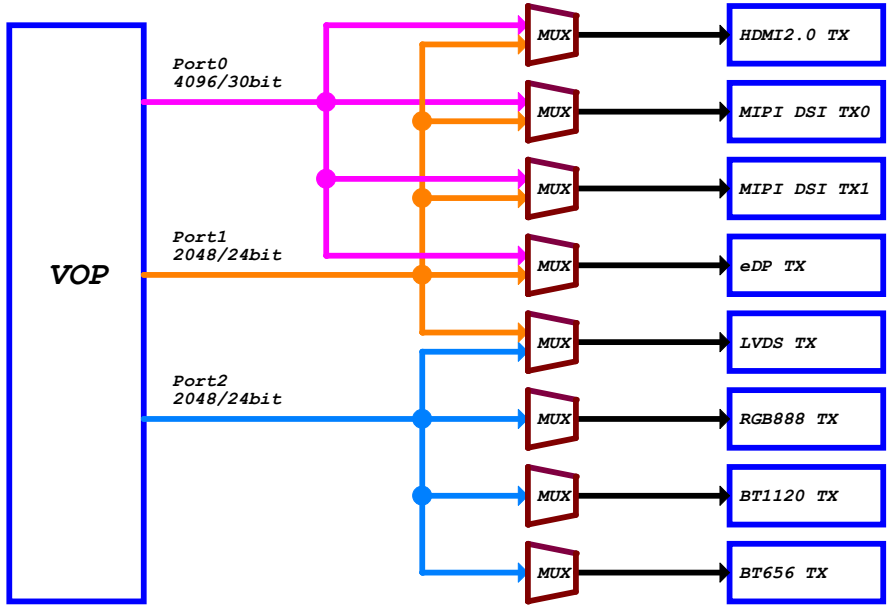
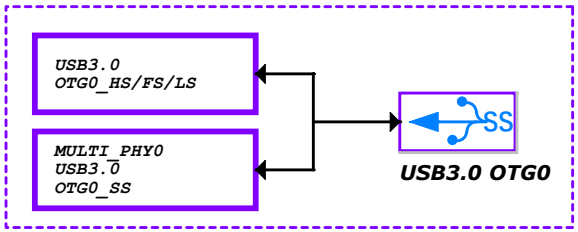
MULTI_PHY0/1/2 Path Map



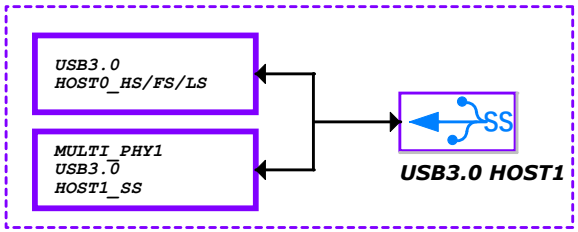
VOP Path Map



USB3.0 OTG0



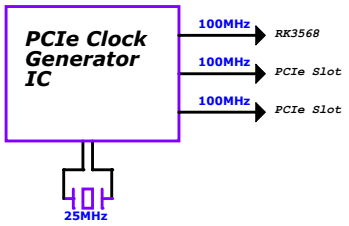
USB3.0 HOST1



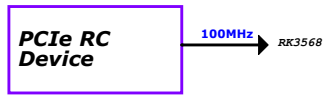
PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

PCIe3.0 REFCLK-RC Mode



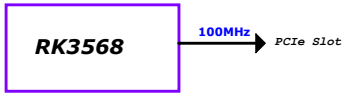
PCIe3.0 REFCLK-EP Mode



PCIe2.1 PHY

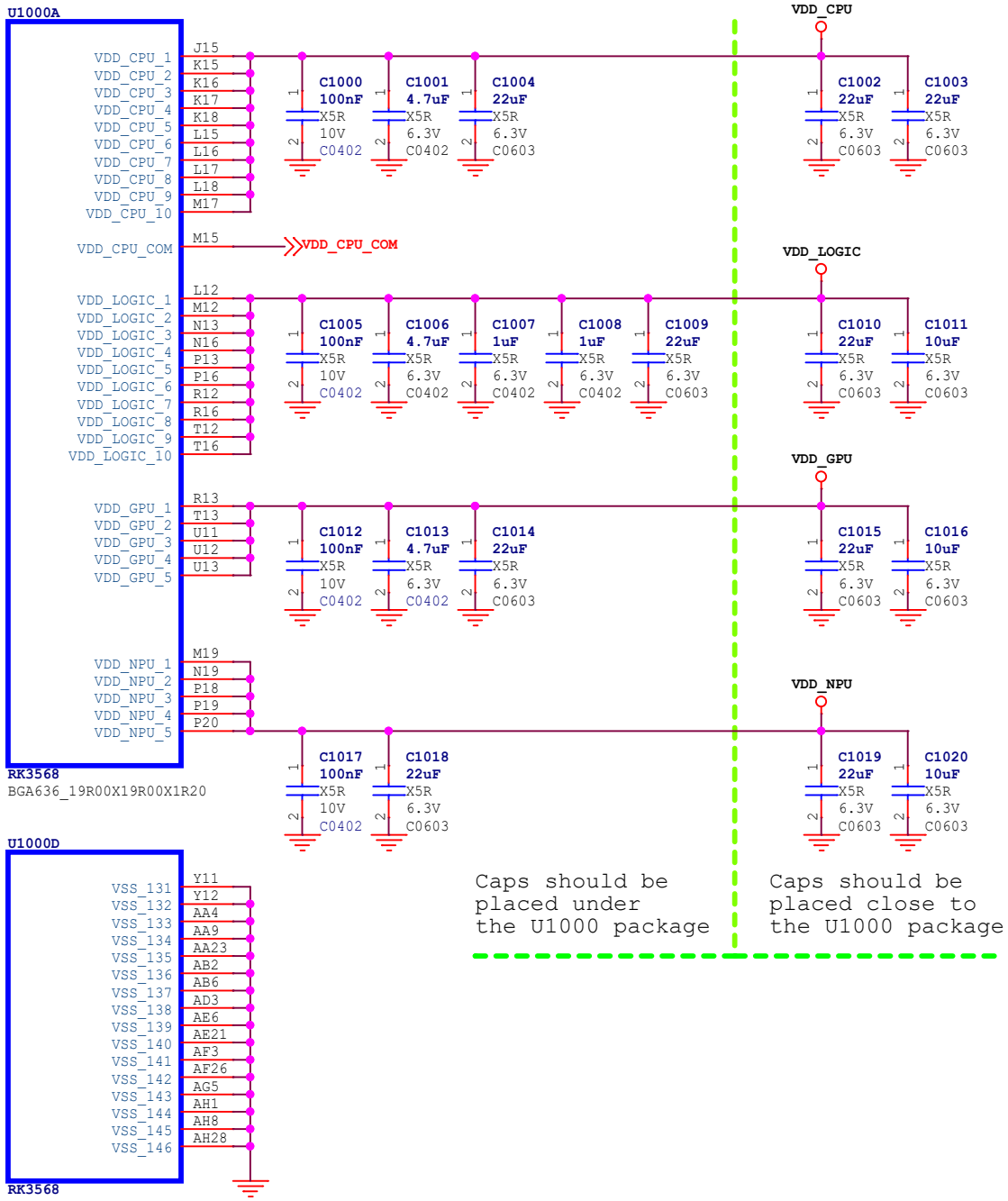
MULTI_PHY2	PCIe2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

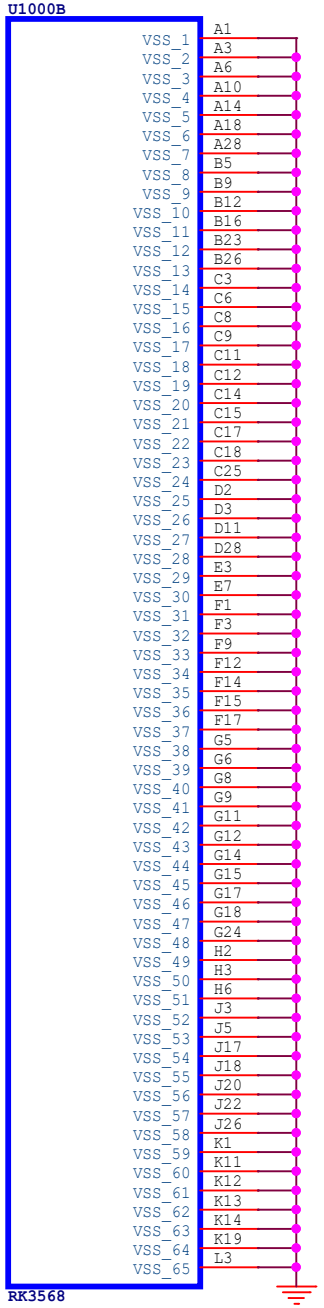
PCIe2.1 REFCLK-RC Mode

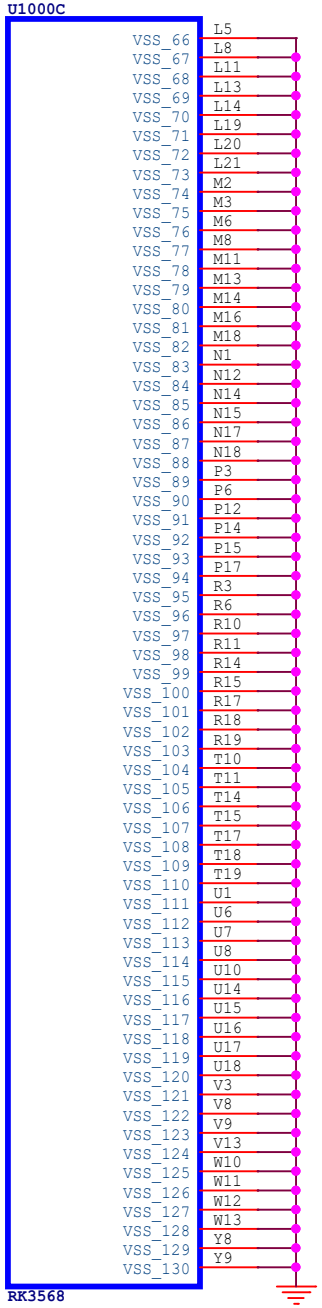


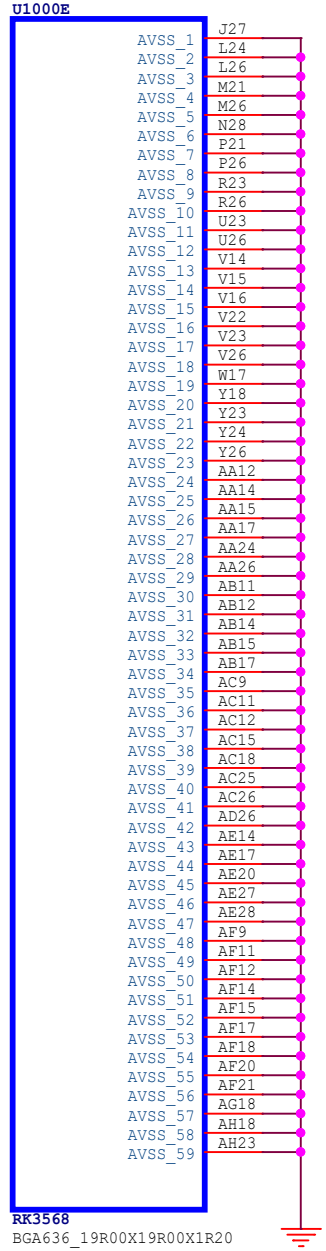
ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	09.PCIE30/MULTI_PHY/VOP Fun Map
Date:	Thursday, May 23, 2024
Rev:	V0.9
Designed by:	Wang
Sheet:	9 of 40

RK3568_ABCDE (Power&Gnd)









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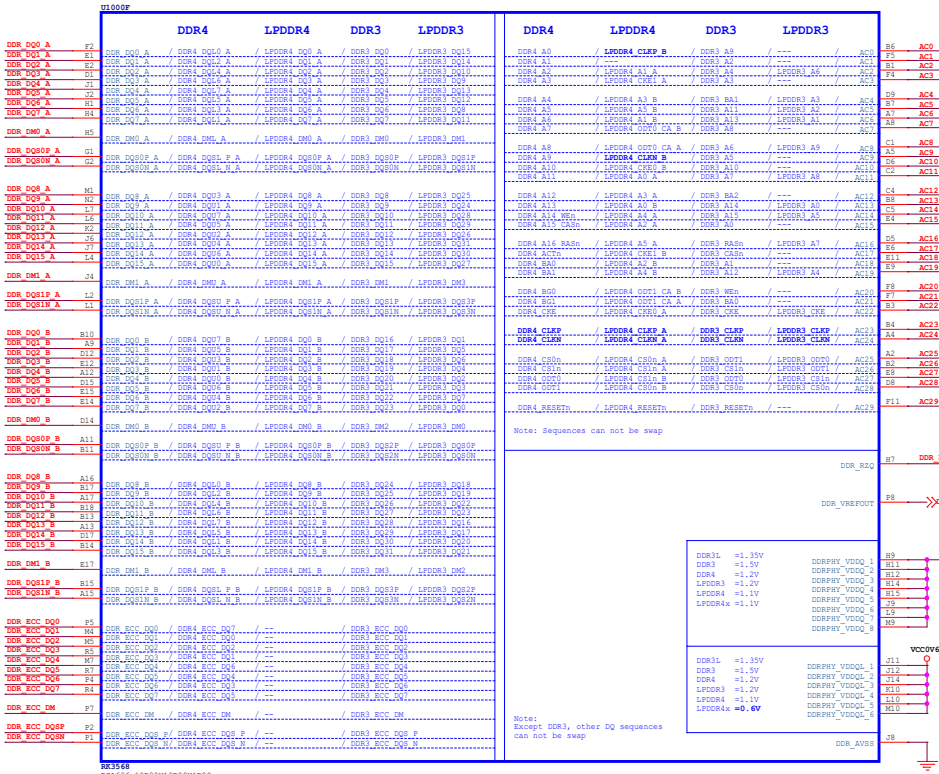
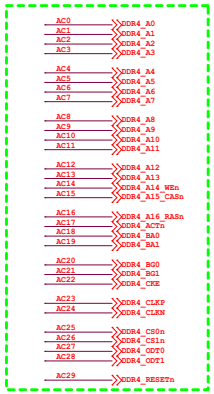
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	10.RK3568_Power/GND		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	10 of 40

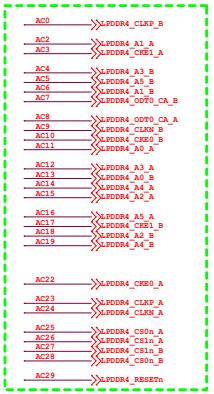
RK3568_F (DDR PHY)



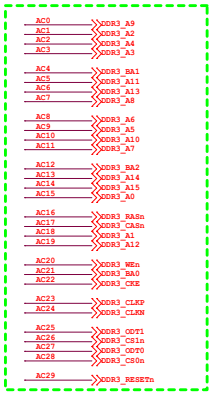
Default DDR4 AC



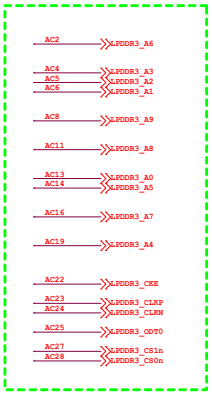
LPDDR4/4x AC



DDR3 AC



LPDDR3 AC

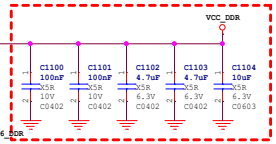


R1100 1 — 2 120R/NC% R0402

R1101 1 — 2 120R 1% R0402

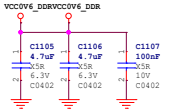
For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin



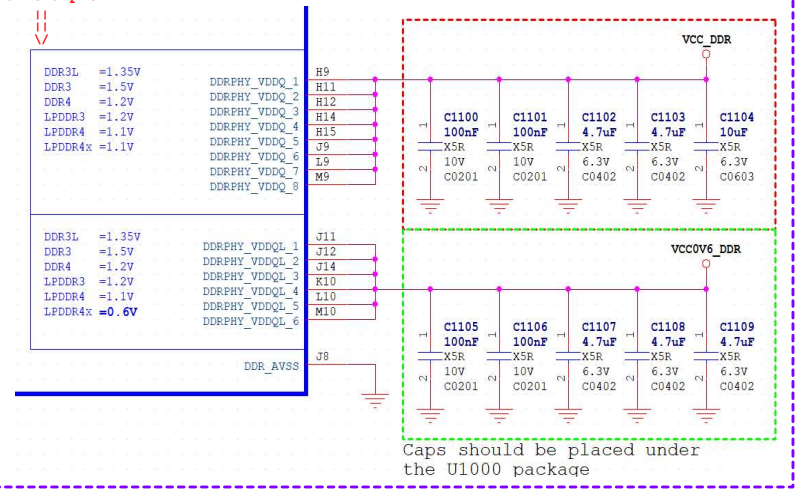
Default DDR4

Note:
Caps should be placed under the U1000 package



Note:

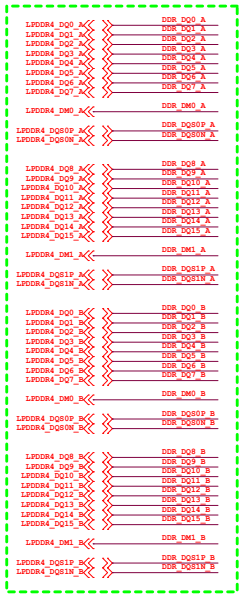
LPDDR4x mode:
Pin J11,J12,J14,K10,L10,M10 connected to VCC0V6_DDR power supply
For example



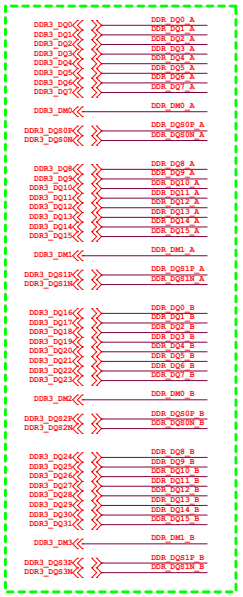
Caps should be placed under the U1000 package

Default DDR4 DQ

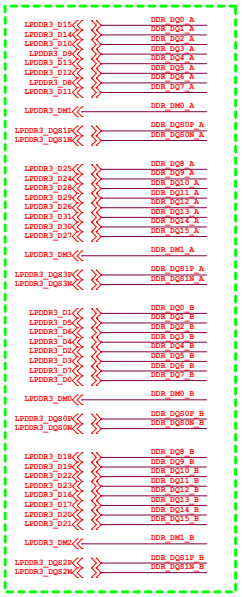
LPDDR4/4x DQ



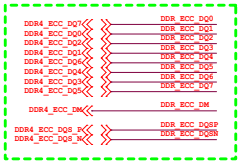
DDR3 DQ



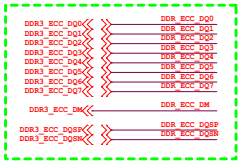
LPDDR3 DQ



DDR4 ECC DQ



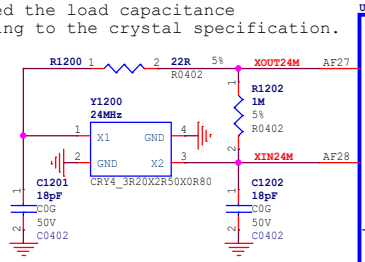
DDR3 ECC DQ

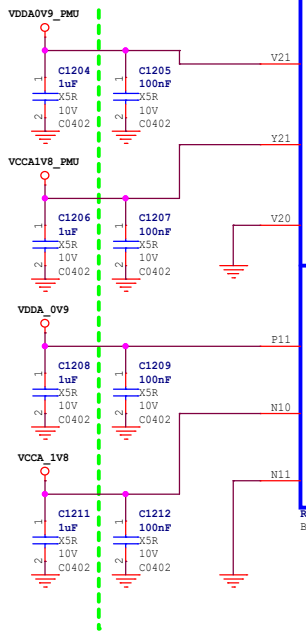


ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	11.RK3568_DDR PHY
Date:	Thursday, May 23, 2024
Rev:	V0.9
Designed by:	Wang
Sheet:	11 of 40

RK3568_G(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification.





U1000G

OSC
XOUT24M
XIN24M

PMUIO0 Domain
Operating Voltage =1.8V(PMUPLL_AVDD_1V8)

TVSS
GPIO0_D3_d
GPIO0_D4_d
GPIO0_D5_d
GPIO0_D6_d
RTCIC_INT_L_GPIO0_D3
PCIE_PWREN_H_GPIO0_D4
AB24
AE26
AB23
AD25
AC24

PMU PLL
PMUPLL_AVDD_0V9
PMUPLL_AVDD_1V8
PMUPLL_AVSS

SYS PLL
SYSPLL_AVDD_0V9
SYSPLL_AVDD_1V8
SYSPLL_AVSS

RK3568
BGA636_19R00X19R00X1R20

PMUIO1 Domain
Operating Voltage=3.3V Only

NPOR_u
REFCLK_OUT / GPIO0_A0_d
TSADC_SHUT_ORG / GPIO0_A1_d
TSADC_SHUT_M0 / GPIO0_A2_d
PMIC_SLEEP / TSADC_SHUT_M1 / GPIO0_A3_u
SDMMC0_DET / SATA_CP_DET / PCIE30X1_CLKREQn_M0 / GPIO0_A4_u
SDMMC0_PWREN / SATA_MP_SWITCH / PCIE20_CLKREQn_M0 / GPIO0_A5_d
GPU_PWREN / SATA_CP_POD / PCIE30X2_CLKREQn_M0 / GPIO0_A6_d
FLASH_VOL_SEL / GPIO0_A7_u
PMUIO1

PMUIO2 Domain
Operating Voltage=1.8V/3.3V

CLK32K_IN / CLK32K_OUT0 / PCIE30X2_BUTTONRSTn / GPIO0_B0_u
I2C0_SCL / GPIO0_B1_u
I2C0_SDA / GPIO0_B2_u
I2C1_SCL / CAN0_TX_M0 / PCIE30X1_BUTTONRSTn / MCU_JTAG_TDO / GPIO0_B3_u
I2C1_SDA / CAN0_RX_M0 / PCIE20_BUTTONRSTn / MCU_JTAG_TCK / GPIO0_B4_u
I2C2_SCL_M0 / SPI1_CLK_M0 / PCIE20_WAKEn_M0 / PWM1_M1 / GPIO0_B5_u
I2C2_SDA_M0 / SPI1_MOSI_M0 / PCIE20_PERSTn_M0 / PWM2_M1 / GPIO0_B6_u
PWM0_M0 / CPUAVS / GPIO0_B7_d
PWM1_M0 / GPUAVS / UART0_RX / GPIO0_C0_d
PWM2_M0 / NPUAVS / UART0_TX / MCU_JTAG_TDI / GPIO0_C1_d
PWM3_IR / EDP_HPDIN_M1 / PCIE30X1_WAKEn_M0 / MCU_JTAG_TMS / GPIO0_C2_d
PWM4 / VOP_PWM_M0 / PCIE30X1_PERSTn_M0 / MCU_JTAG_TRSTn / GPIO0_C3_d
PWM5 / SPI0_CS1_M0 / UART0_RTSn / GPIO0_C4_d
PWM6 / SPI0_MISO_M0 / PCIE30X2_WAKEn_M0 / GPIO0_C5_d
PWM7_IR / SPI0_CS0_M0 / PCIE30X2_PERSTn_M0 / GPIO0_C6_d
HDMITX_CEC_M1 / PWM0_M1 / UART0_CTSn / GPIO0_C7_d
UART2_RX_M0 / GPIO0_D0_u
UART2_TX_M0 / GPIO0_D1_u
PMUIO2

PMUIO1/2/OSC Domain Logic Power
Operating Voltage=0.9V
PMU_VDD_LOGIC_0V9

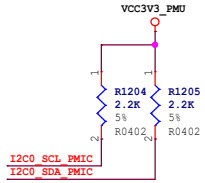
AH27 C1200 100nF X5R 10V C0402 RESETn
R1201 1 2 0R 5% R0402 TSADC_SHUT_M0

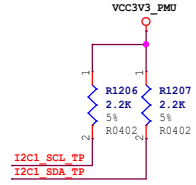
AG27 REFCLKOUT REFCLK_OUT Default:24MHz
AG26 TSADC_SHUT_M0
AG28 PMIC_SLEEP_H
AA22 PMIC_INT_L
Y22 SDMMC0_DET_L
AF25 USB_OTG_PWREN_H_GPIO0_A5
AE24 USB_HOST_PWREN_H_GPIO0_A6
AG25 FLASH_VOL_SEL

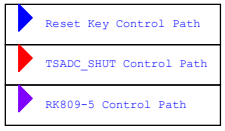
Y20 C1203 100nF X5R 10V C0402 VCC3V3_PMU

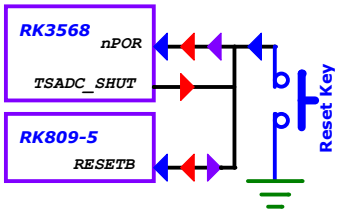
AD23 Power_LED
AF24 I2C0_SCL_PMIC
AB21 I2C0_SDA_PMIC
AG24 I2C1_SCL_TP
AB20 I2C1_SDA_TP
AC22 TP_INT_L_GPIO0_B5
AA20 TP_RST_L_GPIO0_B6
AH26 Working_LEDEN_H_GPIO0_B7
AD22 EDP_HPD
AF23 WIFI_PWREN_L_GPIO0_C1
AG23 PWM3_IR
AE23 LCD0_BL_PWM4
AD21 Dog_IN
AC21 GPIO0_C5 4G_PW_EN
AD20 Dog_EN
AH25 LCD0_PWREN_H_GPIO0_C7
AC20 UART2_RX_M0_DEBUG
AH24 UART2_TX_M0_DEBUG

W19 C1210 100nF X5R 10V C0402 VCC3V3_PMU
V19 C1213 100nF X5R 10V C0402 C1214 1uF X5R 10V C0402 VDDA0V9_PMU









Note:
If PMUIO2 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the PMUIO2 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of PMUIO2 will be abnormally.

The PMUIO2 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of PMUIO2 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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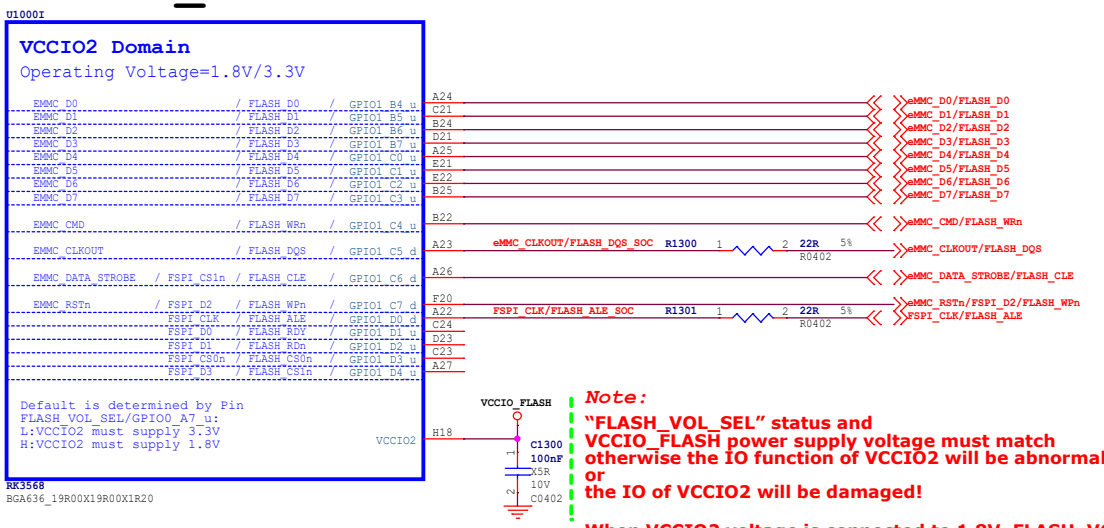
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	12.RK3568_OSC/PLL/PMUIO		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	12 of 40

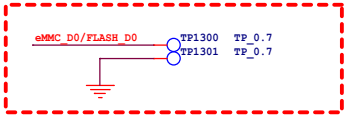
RK3568_I(VCCIO2 Domain)



Note:

"FLASH_VOL_SEL" status and
VCCIO_FLASH power supply voltage must match
otherwise the IO function of VCCIO2 will be abnormally
or
the IO of VCCIO2 will be damaged!

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship,
its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

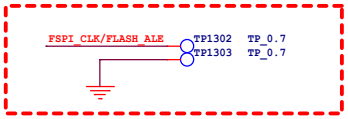


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset,
then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

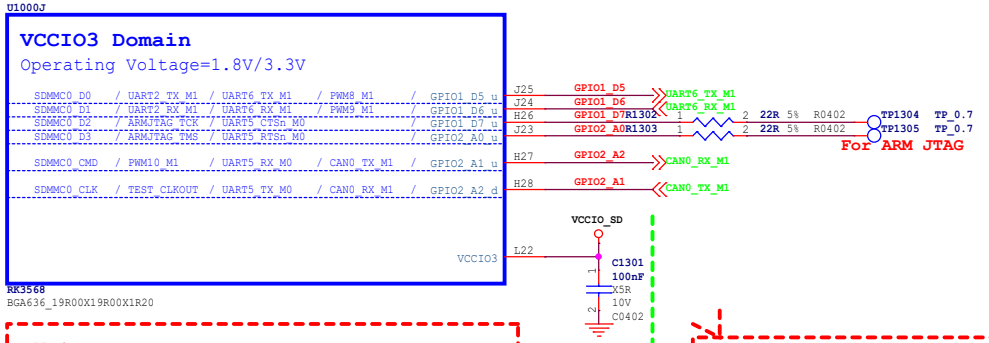
For SPI Flash:
If FSPI_CLK=0V at after power on and reset,
then system will enter into Maskrom mode.

Note:

Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure,
use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:

If VCCIO3 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO3 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO3 will be abnormally.

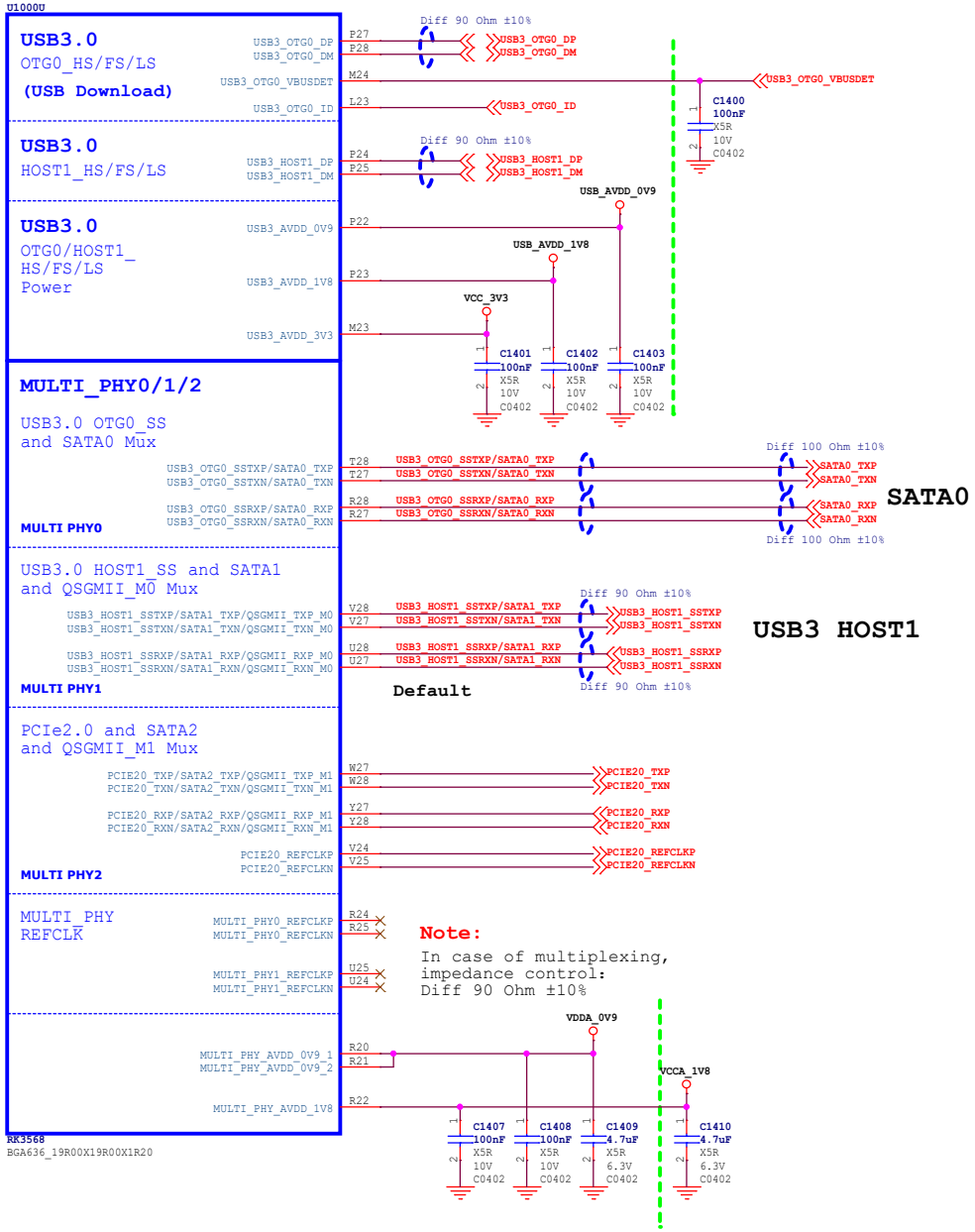
The VCCIO3 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO3 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

UART&CAN&JTAG

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	13.RK3568_Flash/SD Controller		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	13 of 40

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

QSGMII can choose:
QSGMII_TXP_M0/QSGMII_TXN_M0
QSGMII_RXP_M0/QSGMII_RXN_M0
or
QSGMII_TXP_M1/QSGMII_TXN_M1
QSGMII_RXP_M1/QSGMII_RXN_M1

SGMII can choose:
SGMII_TXP_M0/SGMII_TXN_M0
SGMII_RXP_M0/SGMII_RXN_M0
or
SGMII_TXP_M1/SGMII_TXN_M1
SGMII_RXP_M1/SGMII_RXN_M1

See "07.UART Map/GMAC0/1 Path Map"
GMAC0/1 Path Map

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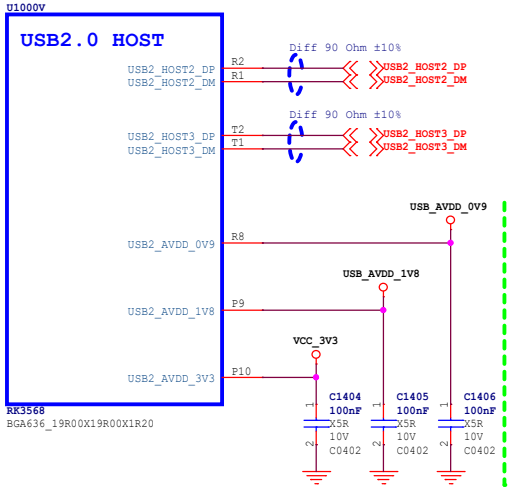
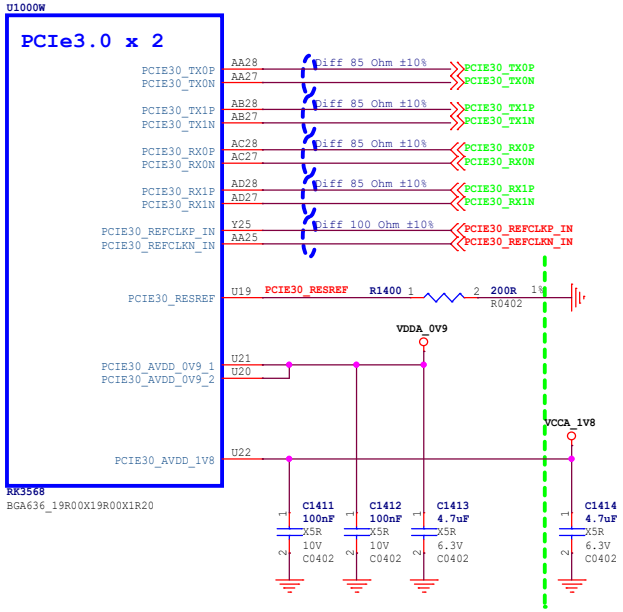
RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	14.RK3568_USB/PCIe/SATA PHY
Date: Thursday, May 23, 2024	Rev: V0.9
Designed by: Wang	Sheet: 14 of 40

RK3568_K(VCCIO4 Domain)

Note: *If VCCIO4 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!*
If the VCCIO4 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO4 will be abnormally.
The VCCIO4 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO4 will be damaged!

Default

WIFI+BT+PCM

U1000K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	GMAC0_RXD2	UART6_RX_M0			GPIO2_A3_u
SDMMC1_D1	GMAC0_RXD3	UART6_TX_M0			GPIO2_A4_u
SDMMC1_D2	GMAC0_RXCLK	UART7_RX_M0			GPIO2_A5_u
SDMMC1_D3	GMAC0_TXD2	UART7_TX_M0			GPIO2_A6_u
SDMMC1_CMD	GMAC0_TXD3	UART9_RX_M0			GPIO2_A7_u
SDMMC1_CLK	GMAC0_TXCLK	UART9_TX_M0			GPIO2_B0_d
SDMMC1_PWREN	I2C4_SDA_M1	UART8_RTSn_M0	CAN2_RX_M1		GPIO2_B1_d
SDMMC1_DET	I2C4_SCL_M1	UART8_CTSn_M0	CAN2_TX_M1		GPIO2_B2_u
	GMAC0_TXD0	UART1_RX_M0			GPIO2_B3_u
	GMAC0_TXD1	UART1_TX_M0			GPIO2_B4_u
	GMAC0_TXEN	UART1_RTSn_M0	SPI1_CLK_M0		GPIO2_B5_u
	GMAC0_RXD0	UART1_CTSn_M0	SPI1_MISO_M0		GPIO2_B6_u
I2S2_SCLK_RX_M0	GMAC0_RXD1	UART6_RTSn_M0	SPI1_MOSI_M0		GPIO2_B7_d
I2S2_LRCK_RX_M0	GMAC0_RXDV_CRS	UART6_CTSn_M0	SPI1_CS0_M0		GPIO2_C0_d
I2S2_MCLK_M0	ETH0_REFCLKO_25M	UART7_RTSn_M0	SPI1_CLK_M0		GPIO2_C1_d
I2S2_SCLK_TX_M0	GMAC0_MCLKINOUT	UART7_CTSn_M0	SPI2_MISO_M0		GPIO2_C2_d
I2S2_LRCK_TX_M0	GMAC0_MDC	UART9_RTSn_M0	SPI2_MOSI_M0		GPIO2_C3_d
I2S2_SDO_M0	GMAC0_MDIO	UART9_CTSn_M0	SPI2_CS0_M0		GPIO2_C4_d
I2S2_SDI_M0	GMAC0_RXER	UART8_TX_M0	SPI2_CS1_M0		GPIO2_C5_d
CLK32K_OUT1		UART8_RX_M0	SPI1_CS1_M0		GPIO2_C6_d

RK3568
BGA636_19R00X19R00X1R20

E27 GPIO2_A3 — SDMMC1_D0
E28 GPIO2_A4 — SDMMC1_D1
B28 GPIO2_A5 — SDMMC1_D2
C27 GPIO2_A6 — SDMMC1_D3
C28 GPIO2_A7 — SDMMC1_CMD
D27 GPIO2_B0 — R1502 2 22R 5% R0402 — SDMMC1_CLK
D26 GPIO2_B1 — WIFI_REG_ON_H_GPIO2_B1
E25 GPIO2_B2 — WIFI_WAKE_HOST_H_GPIO2_B2
F28 GPIO2_B3 — UART1_RX_M0
G27 GPIO2_B4 — UART1_TX_M0
G28 GPIO2_B5 — UART1_RTSn_M0
F27 GPIO2_B6 — UART1_CTSn_M0
H25 GPIO2_B7 — BT_REG_ON_H_GPIO2_B7
F24 GPIO2_C0 — BT_WAKE_HOST_H_GPIO2_C0
G23 GPIO2_C1 — HOST_WAKE_BT_H_GPIO2_C1
F25 GPIO2_C2 — SOC_PCM_CLK
H24 GPIO2_C3 — SOC_PCM_SYNC
H23 GPIO2_C4 — SOC_PCM_OUT
F26 GPIO2_C5 — SOC_PCM_IN
E26

VCCIO4
J21 — R1510 1 2 0R 5% R0402 — VCCIO_WL
C1500 100nF X5R 10V C0402

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

RK3568_N(VCCIO7 Domain)

Note:
When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

U1000N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	SPI3_CLK_M1	CAN1_RX_M1	PCIE30X2_CLKREQn_M2	I2S3_MCLK_M1	GPIO4_C2_d
PWM15_IR_M1	SPI3_MOSI_M1	CAN1_TX_M1	PCIE30X2_WAKEn_M2	I2S3_SCLK_M1	GPIO4_C3_d
EDP_HPDIN_M0	SPDIF_TX_M2	SATA2_ACT_LED	PCIE30X2_PERSTn_M2	I2S3_LRCK_M1	GPIO4_C4_d
PWM12_M1	SPI3_MISO_M1	SATA1_ACT_LED	UART9_TX_M1	I2S3_SDO_M1	GPIO4_C5_d
PWM13_M1	SPI3_CS0_M1	SATA0_ACT_LED	UART9_RX_M1	I2S3_SDI_M1	GPIO4_C6_d
HDMITX_SCL	I2C5_SCL_M1				GPIO4_C7_u
HDMITX_SDA	I2C5_SDA_M1				GPIO4_D0_u
HDMITX_CEC_M0	SPI3_CS1_M1				GPIO4_D1_u
					GPIO4_D2_d

RK3568
BGA636_19R00X19R00X1R20

AF8 GPIO4_C2 — GPIO4_C2
AA11 GPIO4_C3 — GPIO4_C3
AH7 GPIO4_C4 — GPIO4_C4
AD8 GPIO4_C5 — GPIO4_C5
AE8 GPIO4_C6 — SATA0_ACT_LED
AG8 — HDMITX_SCL
AG7 — HDMITX_SDA
AH6 — HDMITX_CEC_M0
AB9 — LED3

VCC_3V3
V12 — C1509 100nF X5R 10V C0402 — VCCIO7

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
If VCCIO7 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO7 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO7 will be abnormally.

The VCCIO7 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO7 will be damaged!

RK3568_O(SARADC/OTP)

U1000O

SARADC

Recovery/ SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY	C1501 1 2 1nF X5R 50V C0402
SARADC_VIN1	C26	SARADC_VIN1_HW_ID	C1502 1 2 1nF X5R 50V C0402
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK	C1503 1 2 1nF X5R 50V C0402
SARADC_VIN3	E23	SARADC_VIN3_BOM_ID	C1504 1 2 1nF X5R 50V C0402
SARADC_VIN4	G21	SARADC_VIN4	C1505 1 2 1nF X5R 50V C0402
SARADC_VIN5	F22	SARADC_VIN5	C1506 1 2 1nF X5R 50V C0402
SARADC_VIN6	G20	SARADC_VIN6	C1507 1 2 1nF X5R 50V C0402
SARADC_VIN7	F21	SARADC_VIN7	C1508 1 2 1nF X5R 50V C0402
SARADC_AVDD_1V8	H22		C1510 100nF X5R 10V C0402
OTP_VCC18	H20		C1511 100nF X5R 10V C0402

OTP

RK3568
BGA636_19R00X19R00X1R20

VCCA_1V8
VCC_1V8

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:
Must be mounted

VCCA_1V8 — R1512 10K 1% R0402 — SARADC_VIN0_KEY/RECOVERY

SARADC_VIN0_KEY/RECOVERY — TP1501 TP_0.7
TP1502 TP_0.7

Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1_HW_ID
SARADC_VIN2_HP_HOOK
SARADC_VIN3_BOM_ID
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	15.RK3568_SARADC/GPIO		
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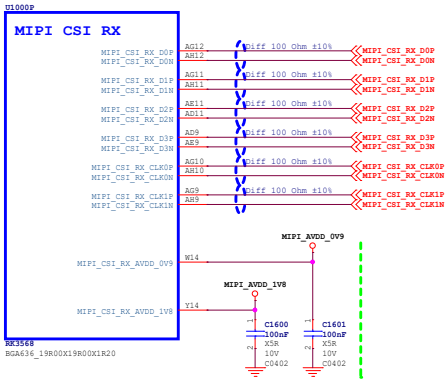
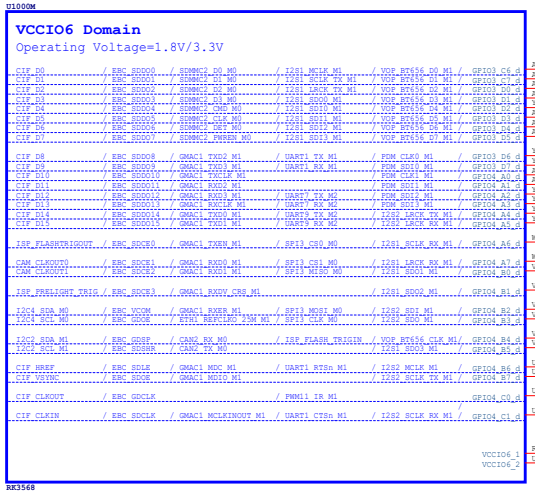
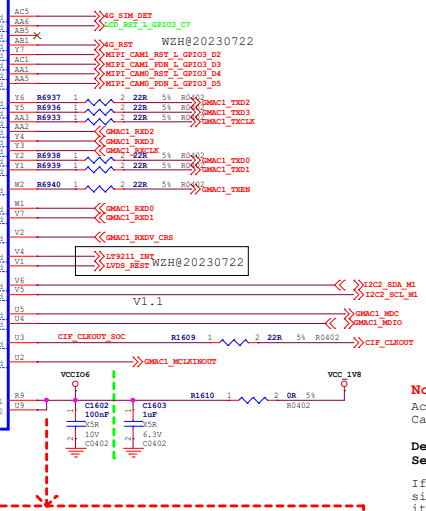
RK3568_P(MIPI_CSI_RX)

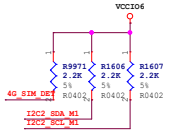


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)







Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If VCCIO6 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO6 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO6 will be abnormally.

The VCCIO6 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO6 will be damaged!

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Default:1.8V
Select the voltage according to the application

If the IO domain is to be used as FEPHY,
since some FEPHY only support 3.3V IO,
it is recommended to reallocate GPIO
to reduce the cost of level conversion

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_CRS_DV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx OSC	ETHx_REFCLKO_25M	------->	PHYx OSC
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	<------->	PHYx_TXC
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	16.RK3568_VI Interface
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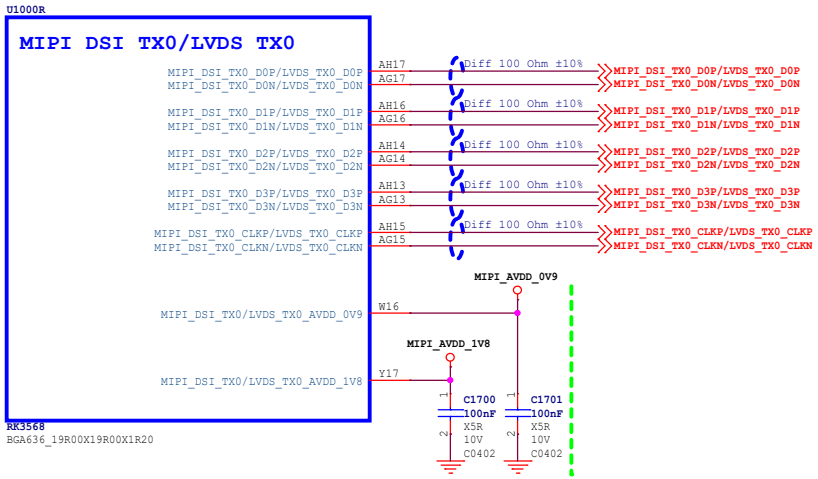
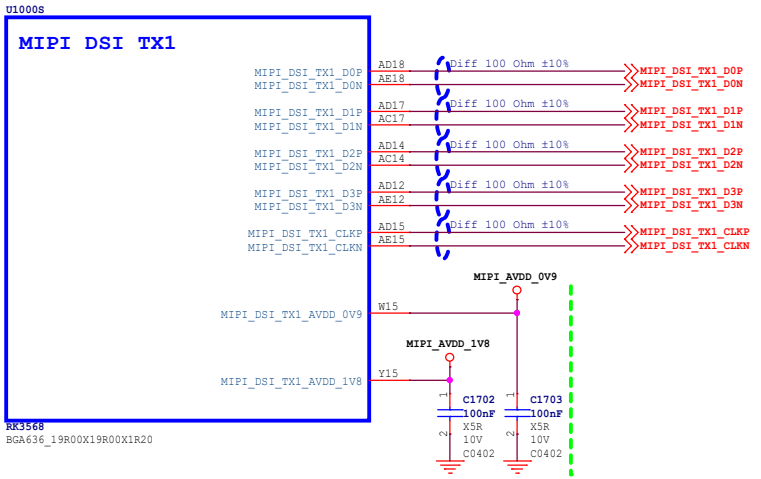
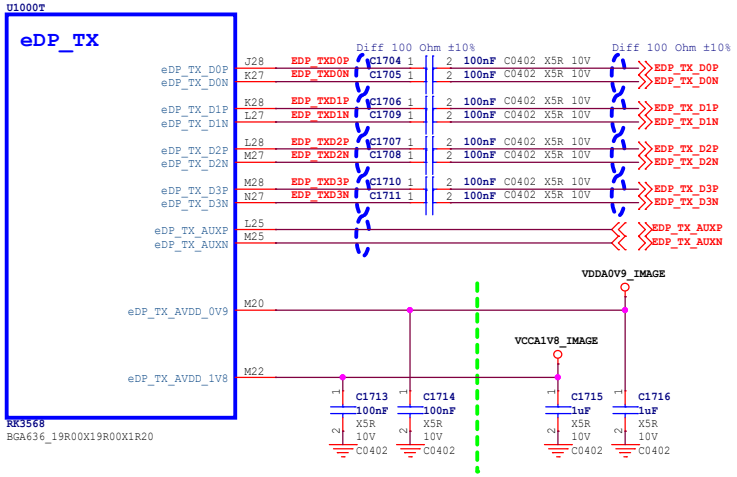
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

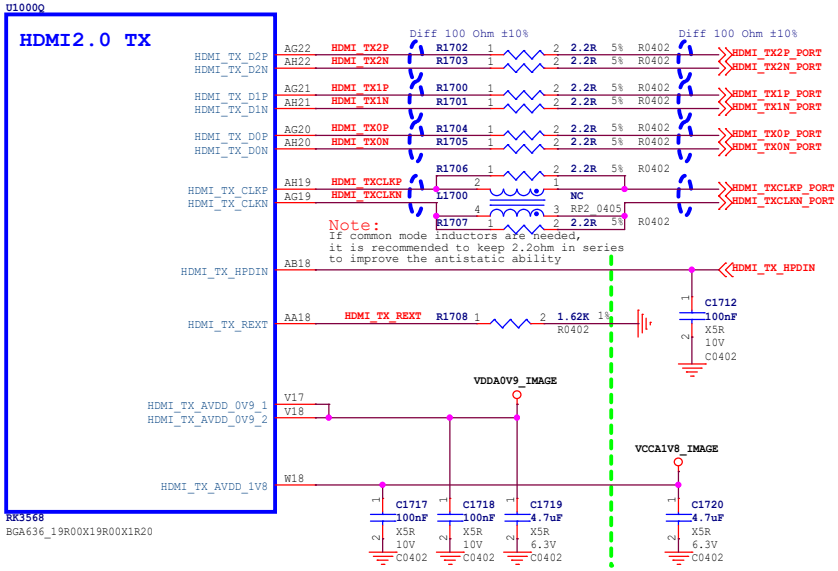


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	17.RK3568_HDMI_LVDS_MIPI_EDP
Date: Thursday, May 23, 2024	Rev: V0.9
Designed by: Wang	Sheet: 17 of 40

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568
BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn_M1
AD7 PCIE20_WAKEn_M1
AC8 RS485_DIR2
AC7 RS485_DIR3
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 UART8_TX_M1
AH4 UART8_RX_M1
AB8 RS485_DIR4
AE5 I2S3_MCLK_M0 — TP1800 TP_0.7
AG4 I2S3_SCLK_M0_SOC — TP1804 TP_0.7
AF4 I2S3_LRCK_M0_SOC — TP1805 TP_0.7
AH3 I2S3_SDO_M0 — TP1801 TP_0.7
AG3 LCD0_EN
AH2 GMAC1_INT/PMEB_GPIO3_A7
AG2 GMAC1_RSTn_L
AG1 UART4_RX_M1
AF2 UART4_TX_M1
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 RS485_DIR_GPIO3_B5
AE3 PCIE_ETH_ISOLATE_L
AD4 GPIO3_B7 UART3_TX_M1
AD2 GPIO3_C0 UART3_RX_M1
AD1 PCIE20_PERSTn_M1
AA7 HP_DET_L_GPIO3_C2
AC4 SPK_CTL_H_GPIO3_C3
AC3 GPIO3_C4 UART7_TX_M1
AC2 GPIO3_C5 UART7_RX_M1

VCC_3V3
V10
V11
C1800 100nF X5R 10V C0402

VCC_3V3
R1801 10K 5% R0402
GMAC1_INT/PMEB_GPIO3_A7
od

VCC_3V3
R1804 2.2K 5% R0402
R1805 2.2K 5% R0402
I2C5_SCL_M0
I2C5_SDA_M0

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
If VCCIO5 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO5 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO5 will be abnormally.

The VCCIO5 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO5 will be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	18.RK3568_VO Interface_2		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	18 of 40

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

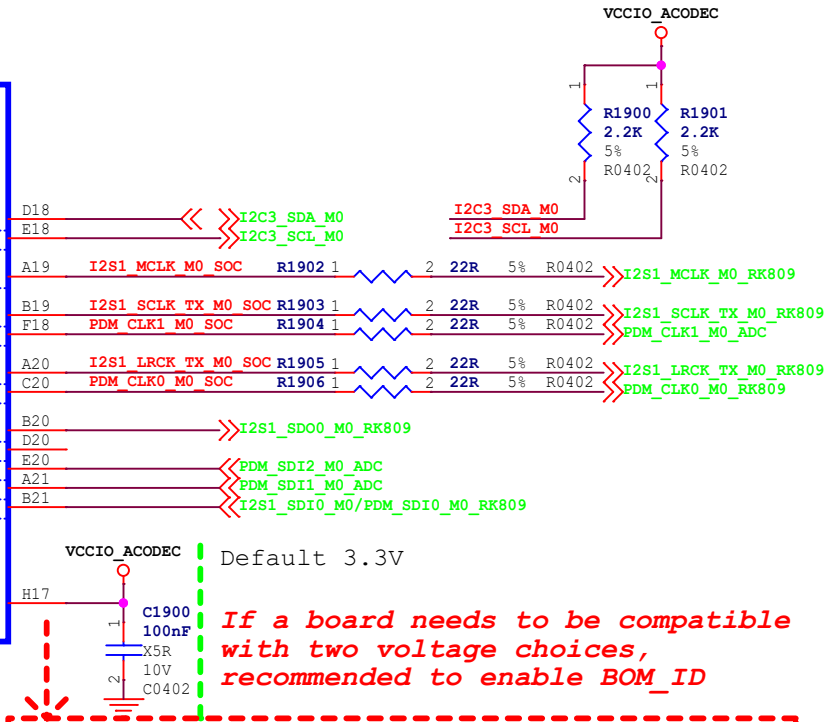
Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0		/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0		/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0				/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20



Note:

If VCCIO1 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO1 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO1 will be abnormally.

The VCCIO1 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO1 will be damaged!

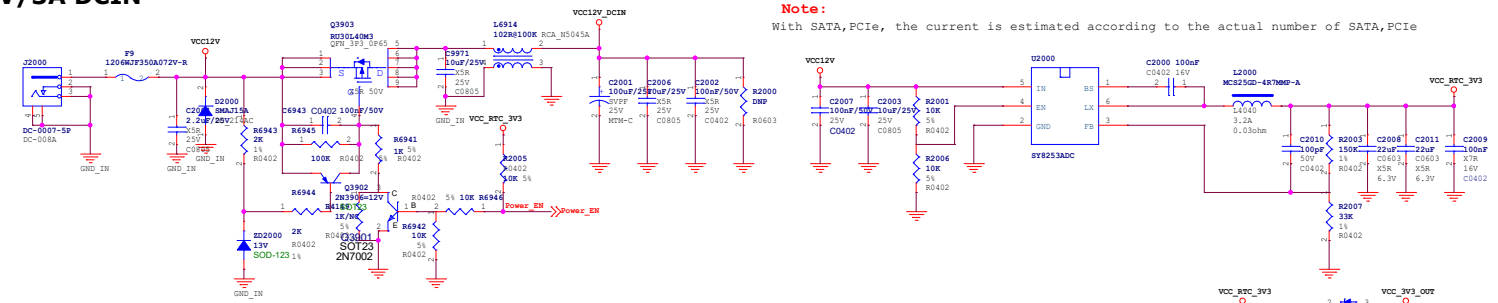
Note:

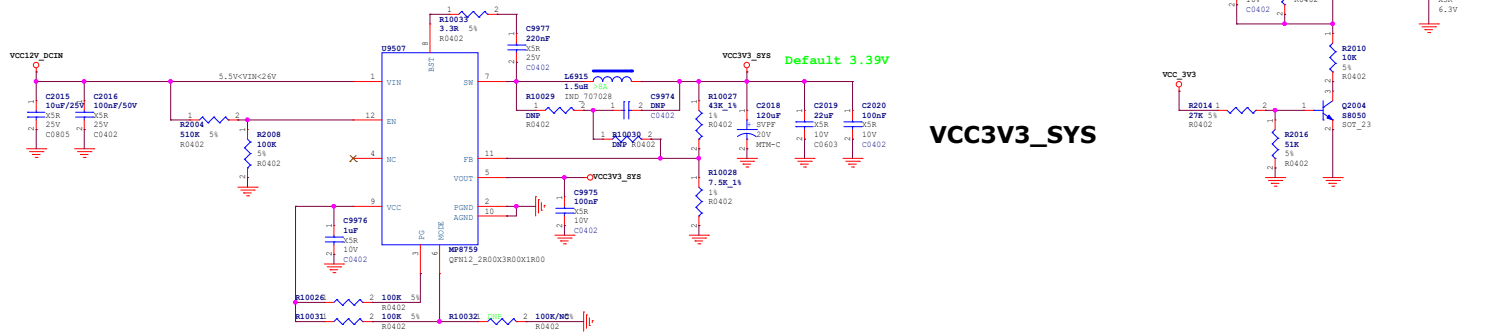
Caps of between dashed green lines and U1000 should be placed under the U1000 package

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	19.RK3568_Audio Interface		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	19 of 40

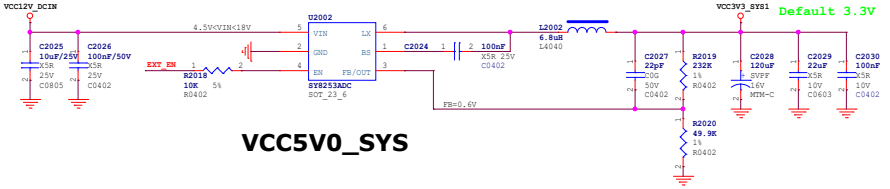
12V/3A DCIN

Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe

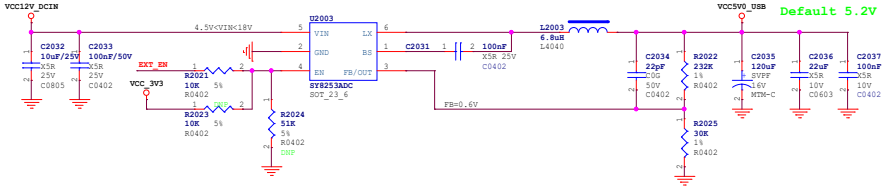




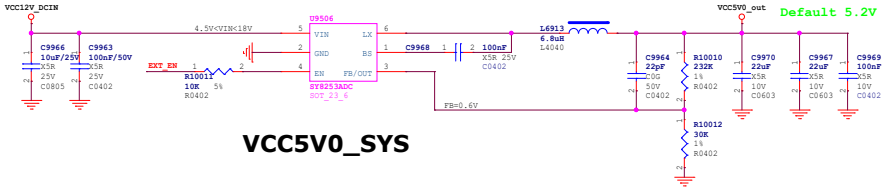
VCC3V3_SYS



VCC5V0_SYS



VCC5V0_USB



VCC5V0_SYS

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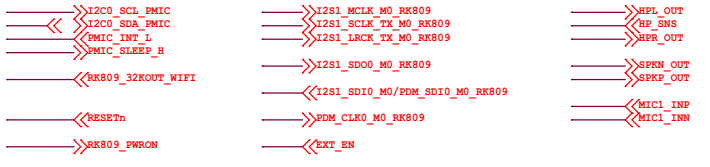
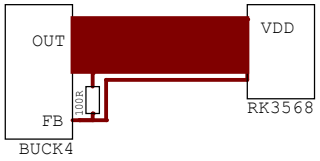
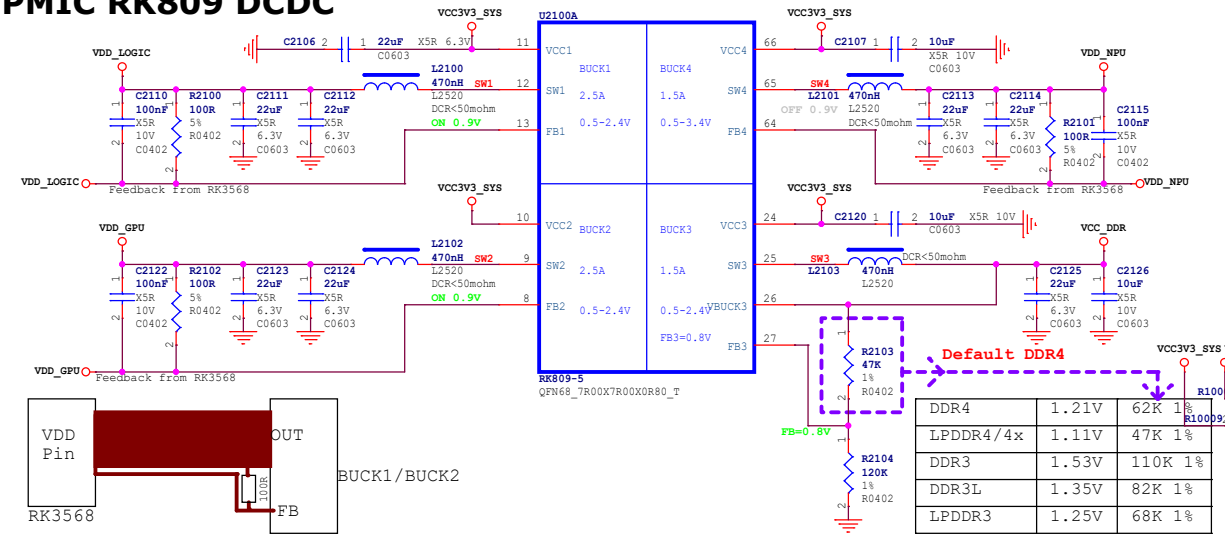
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	20.Power_DC IN		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	20 of 40



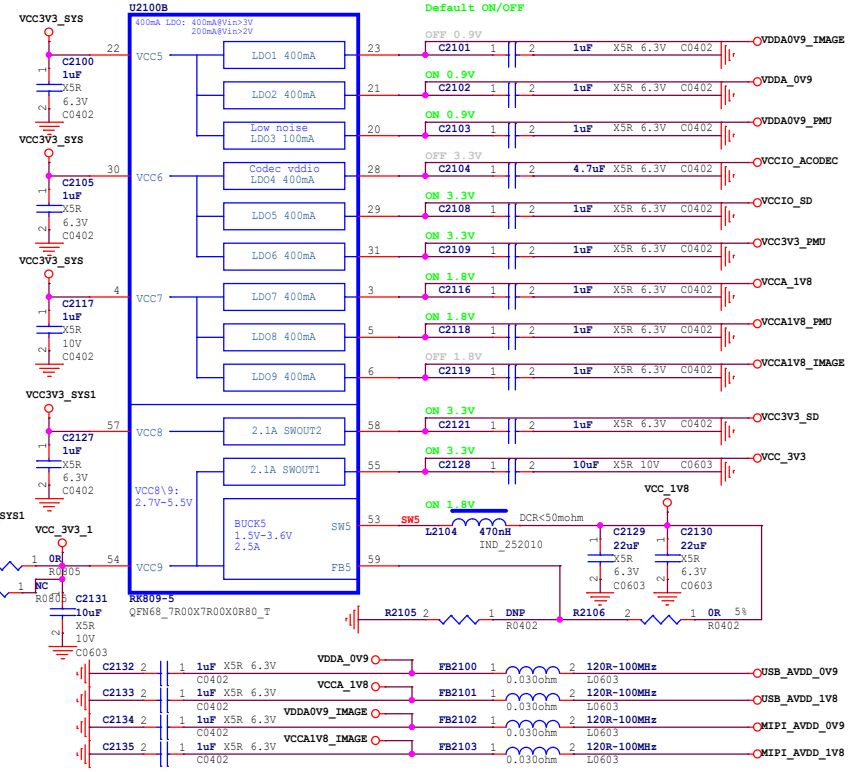


PMIC RK809 DCDC

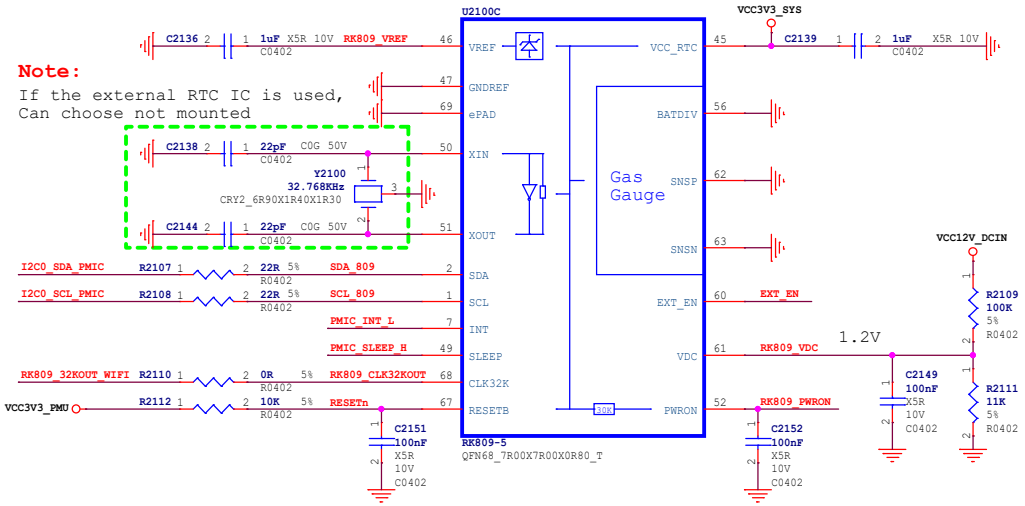


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

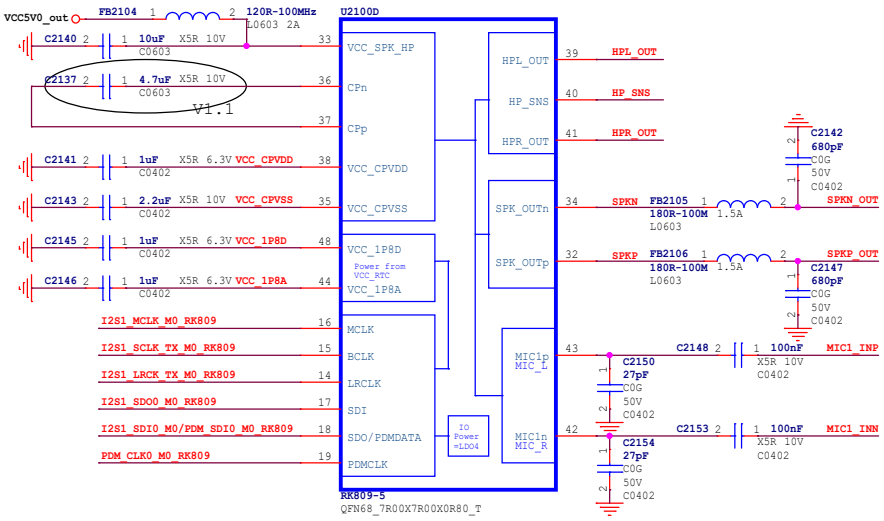
PMIC RK809 LDO



PMIC RK809 Managerment



PMIC RK809 CODEC



Note:

If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	21.Power_PMIC		
Date:	Thursday, May 23, 2024	Rev:	V0.9
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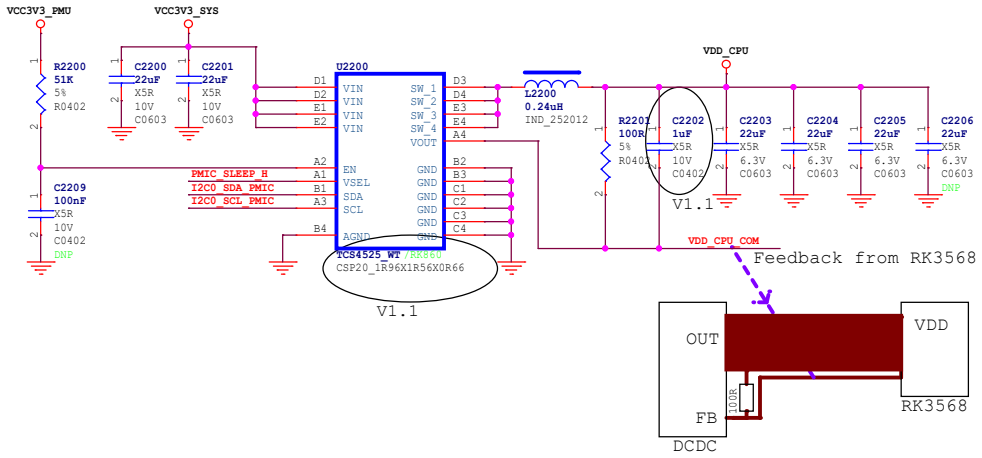
I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_COM

RTCIC_INT_L_GPIO0_D3
RTCIC_32KOUT
I2C5_SCL_M0
I2C5_SDA_M0

VDD_CPU

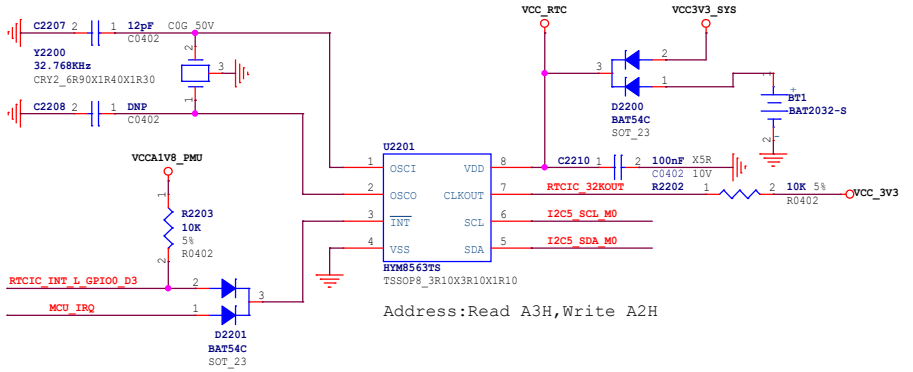


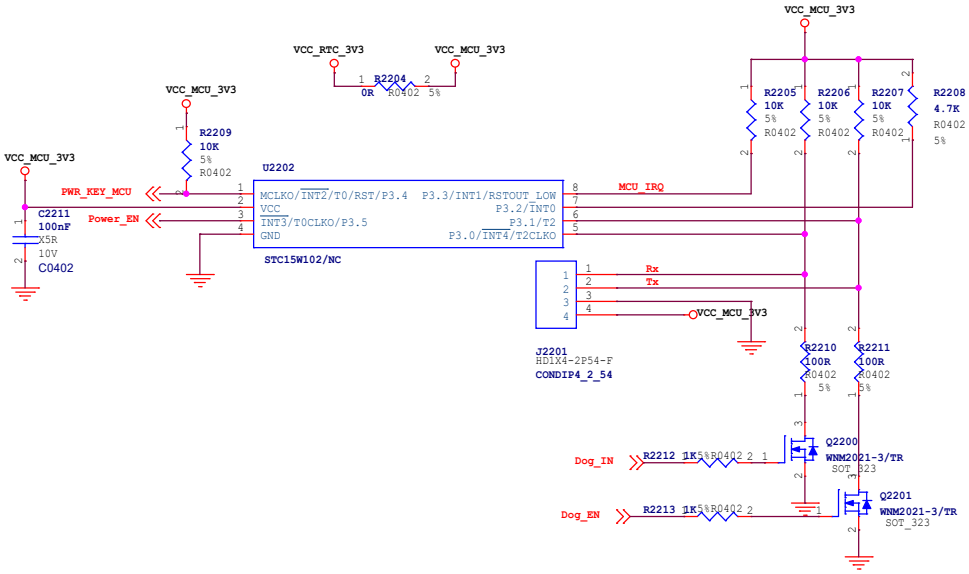
RTC IC --Option

Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC

But, it will not support the timing poweron function





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ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	22.Power_Ext Discrete/RTC IC		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	22 of 40

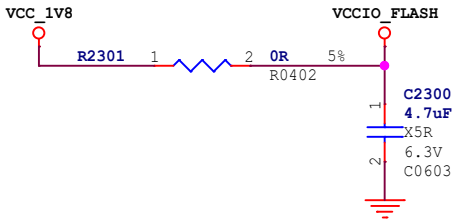
FLASH_VOL_SEL

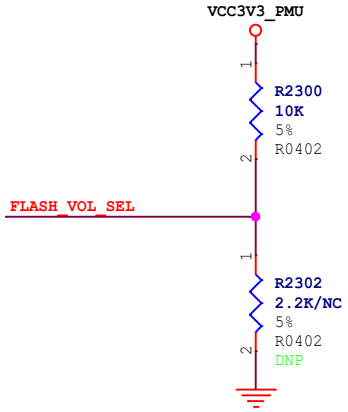
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time



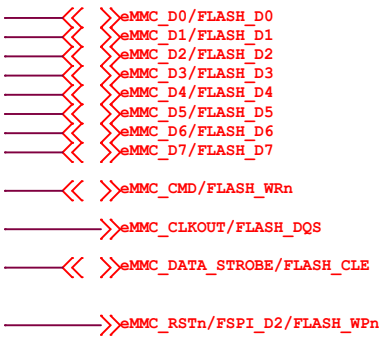


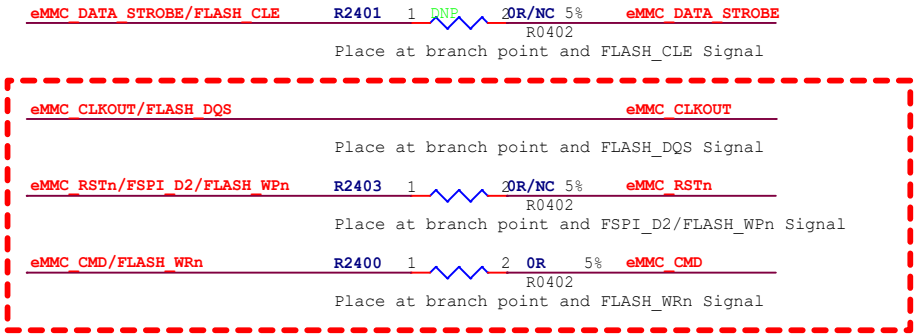
Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship,
its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	23.Power_Flash Power Manage		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	23 of 40

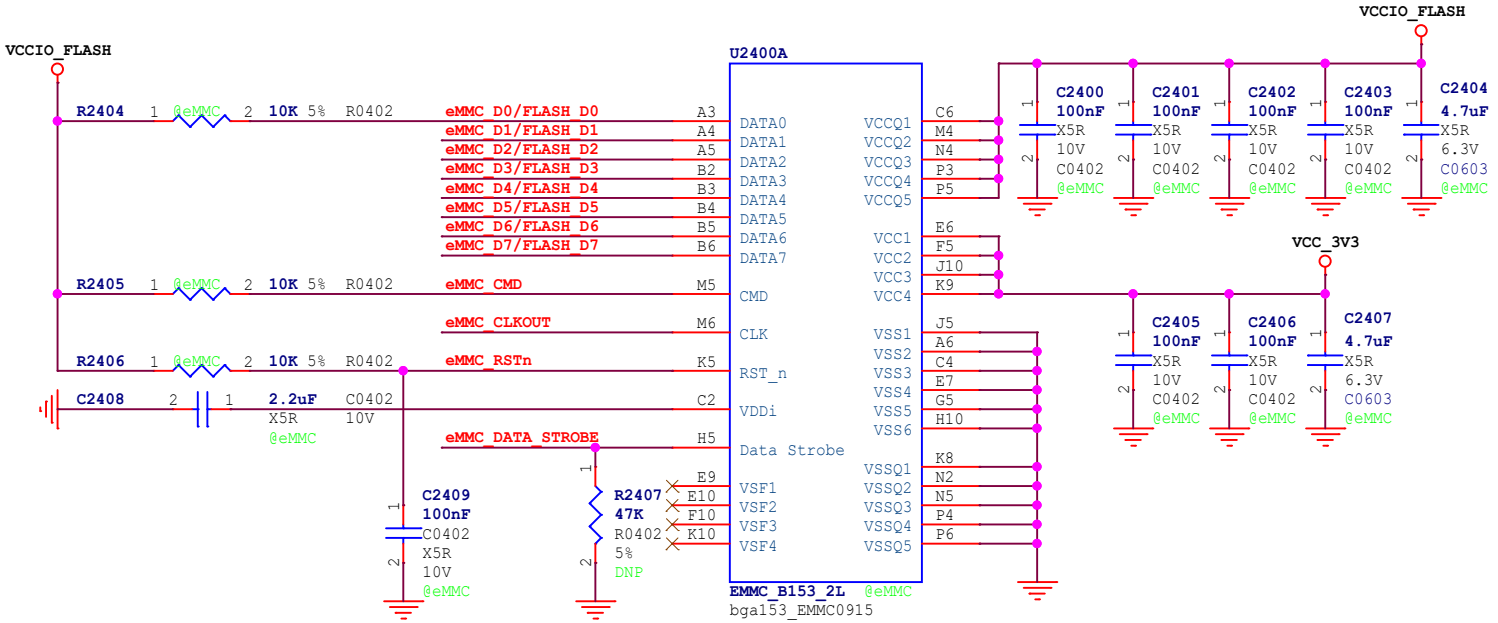
eMMC Flash

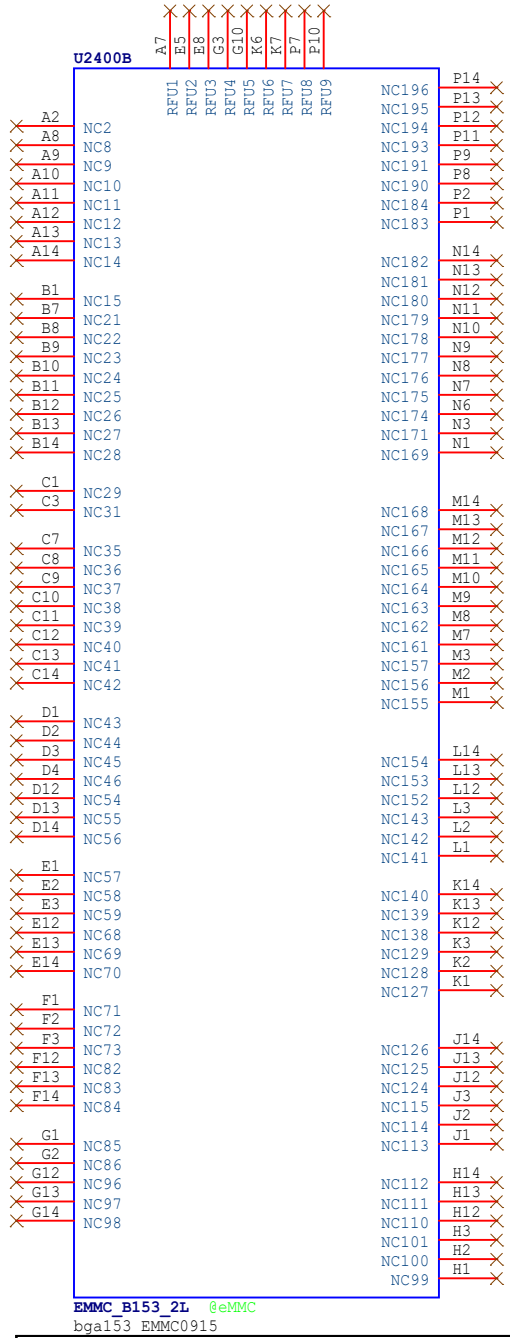




Note:

No need to double layout with Nand Flash, 0R resistor can be omitted





Note:

If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

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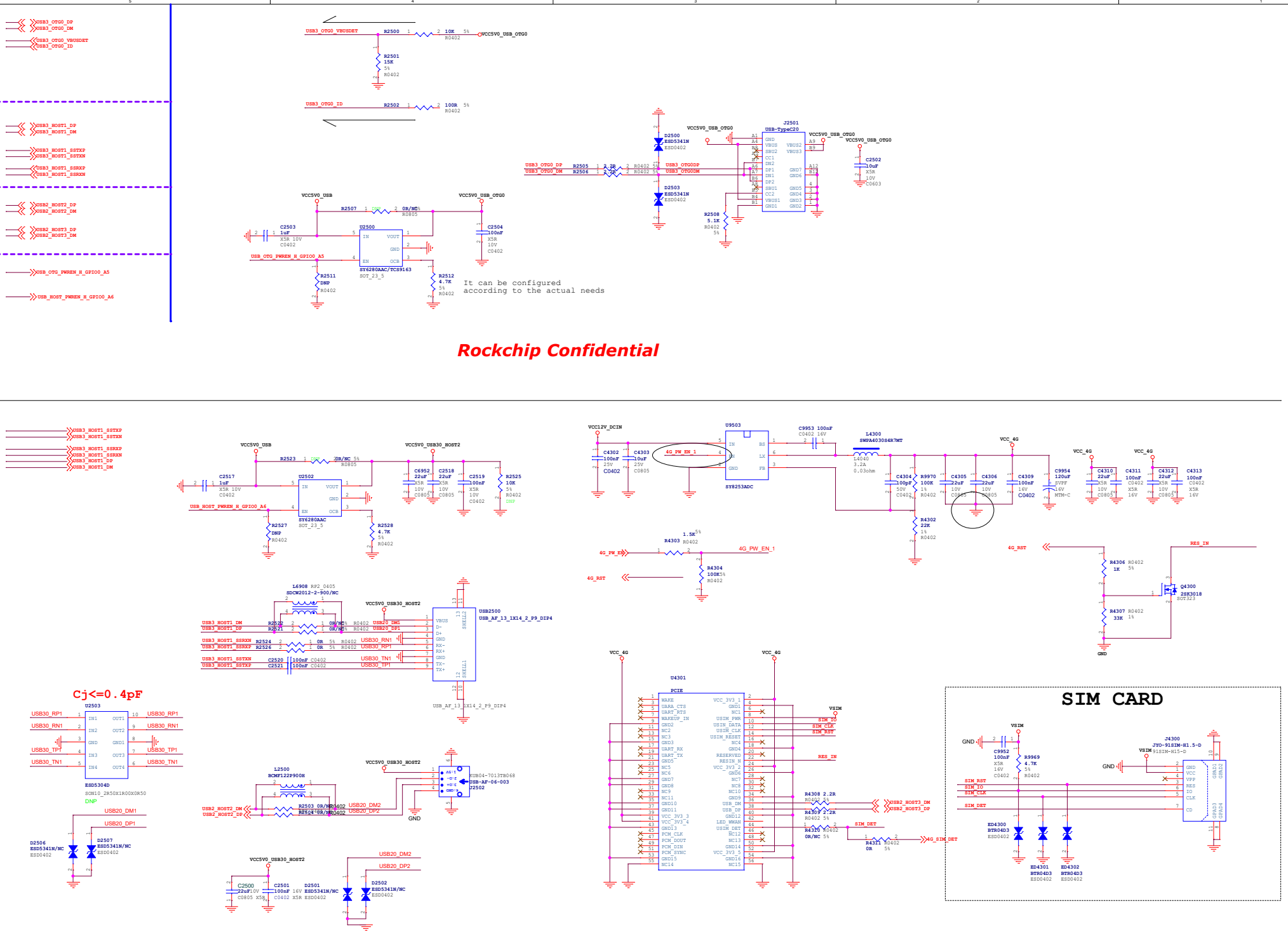
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	24.Flash-eMMC Flash		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	24 of 40



ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	25.USB2/USB3 Port
Date:	Thursday, May 23, 2024
Rev:	V0.9
Designed by:	Wang
Sheet:	25 of 40

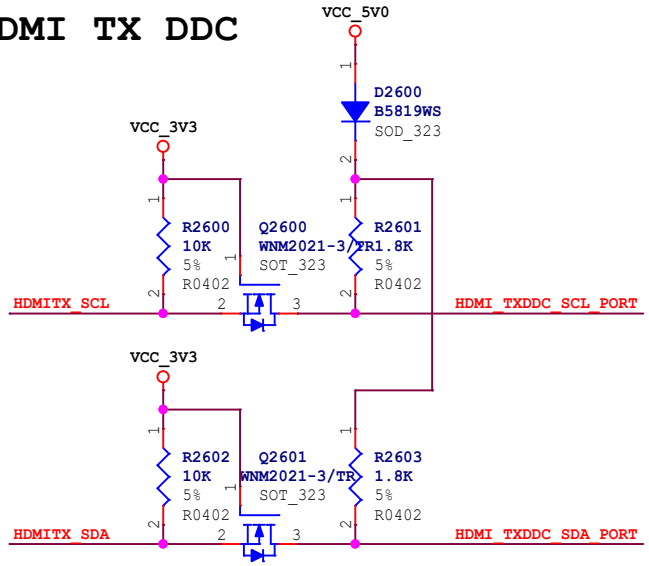
HDMI2.0 TX

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT

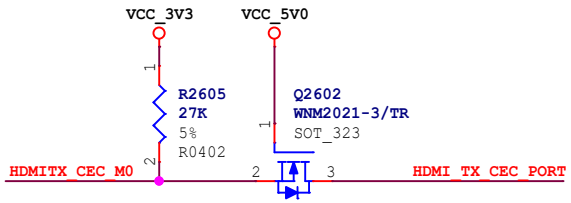
HDMITX_SCL
HDMITX_SDA

HDMITX_CEC_M0
HDMI_TX_HPDIN

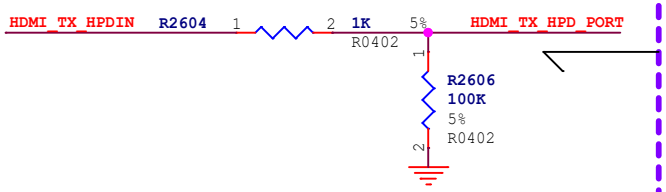
HDMI TX DDC

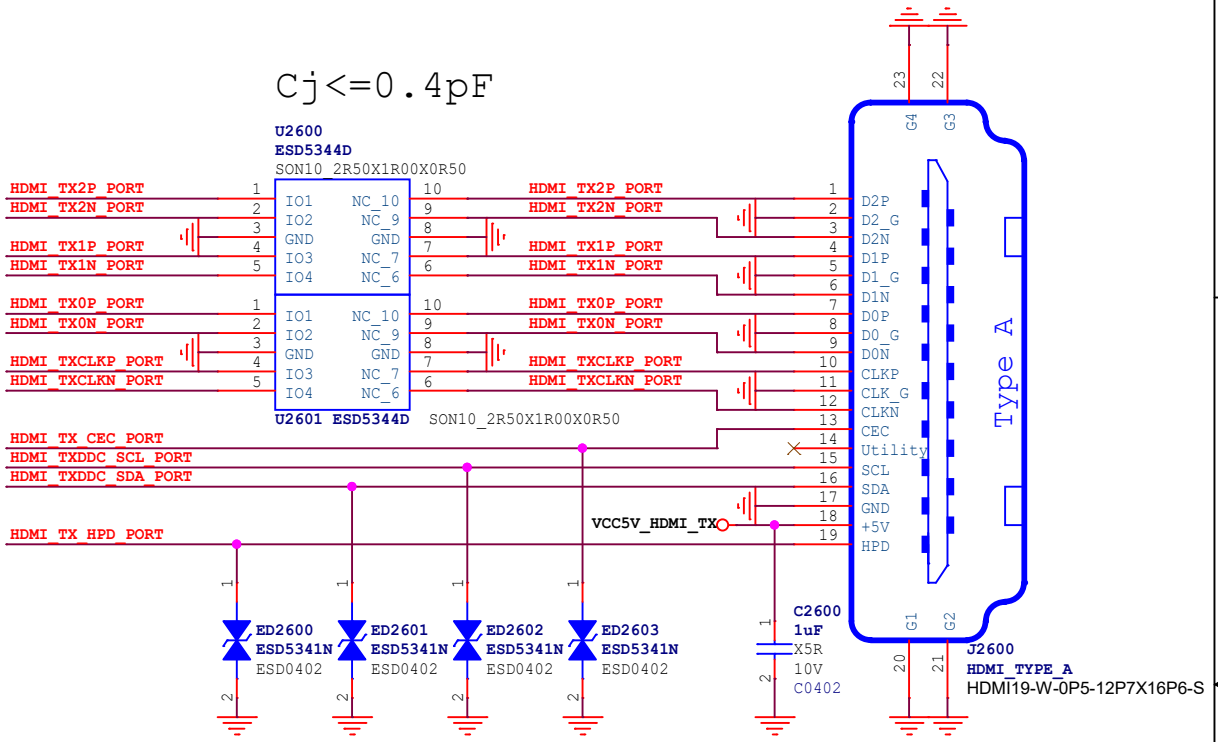


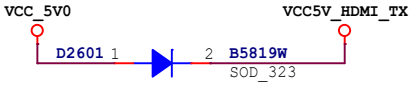
HDMI TX CEC



HDMI TX HPD







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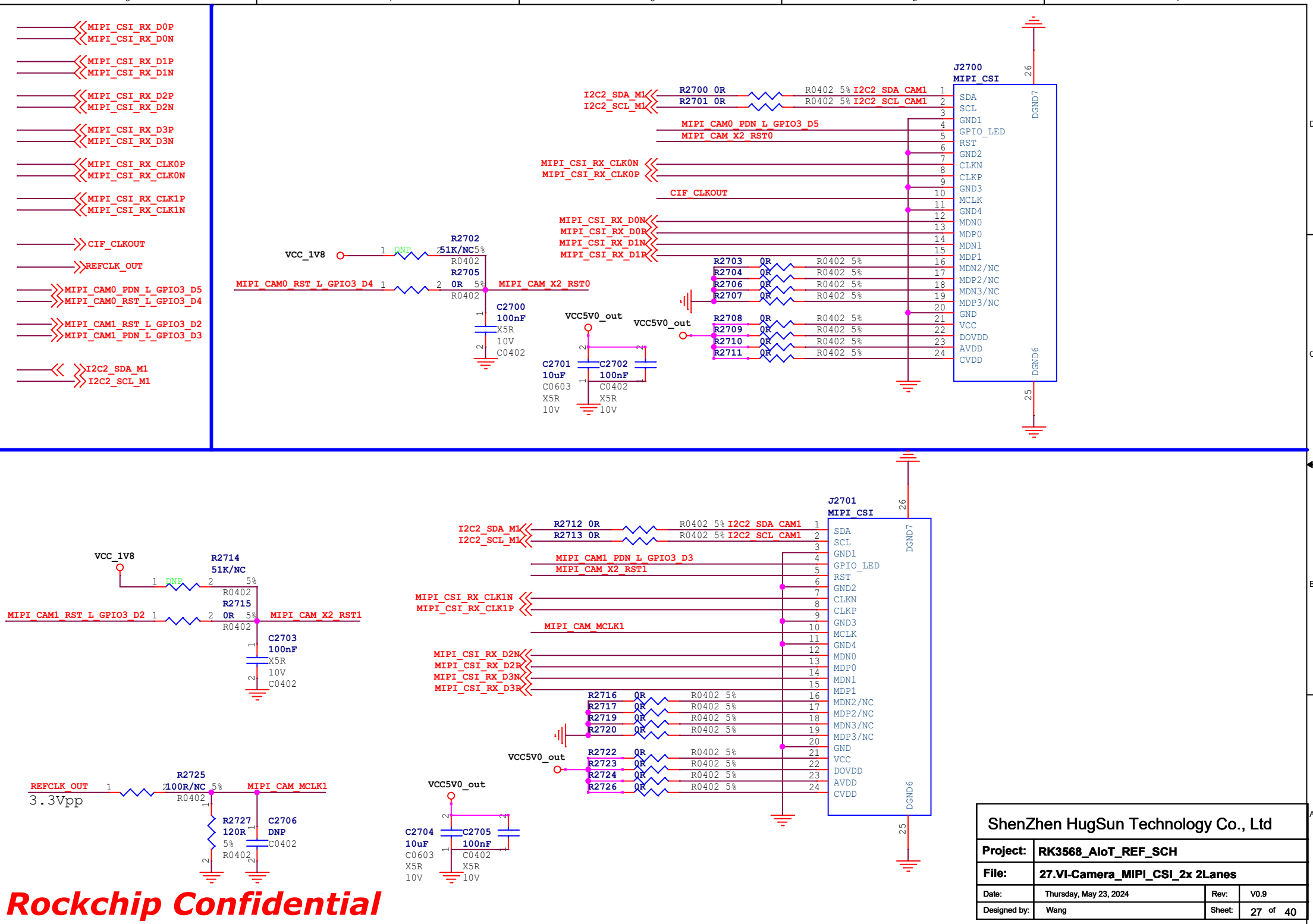
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	26.VO-HDMI2.0 TX		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	26 of 40



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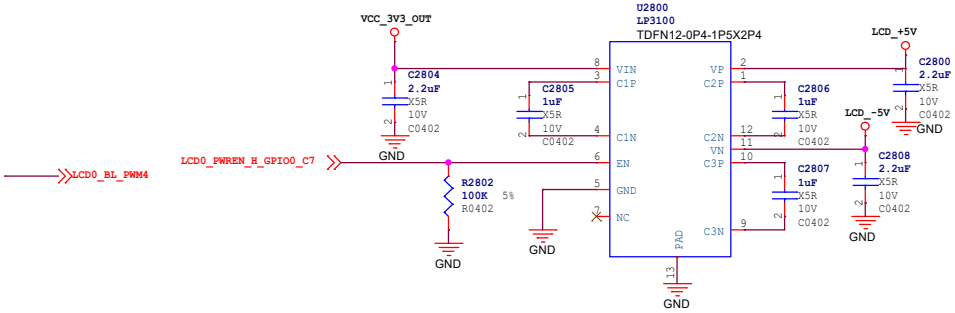
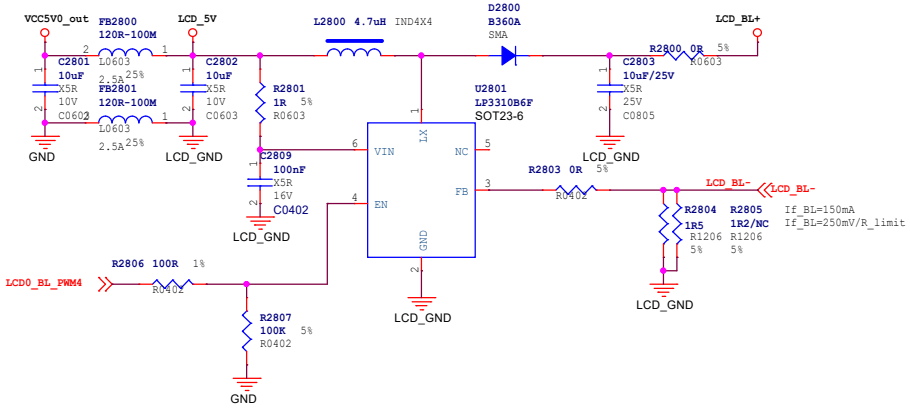
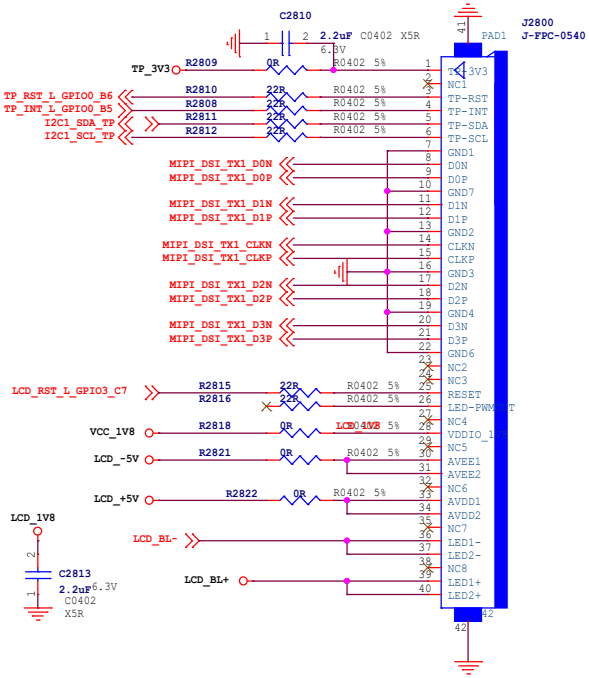
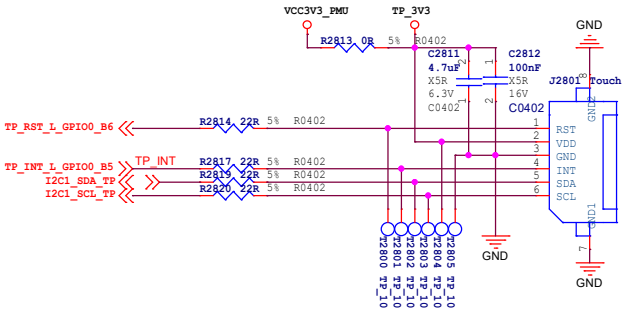
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	27.VI-Camera_MIPI_CSI_2x 2Lanes		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	27 of 40

Single-MIPI0 LCM



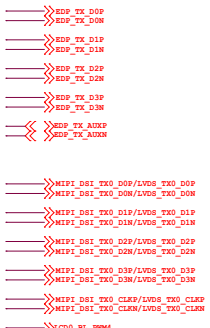




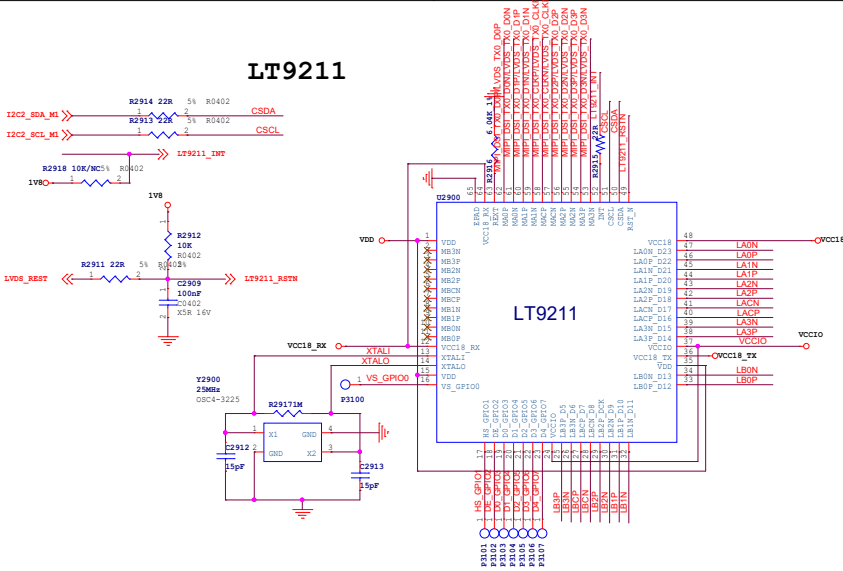


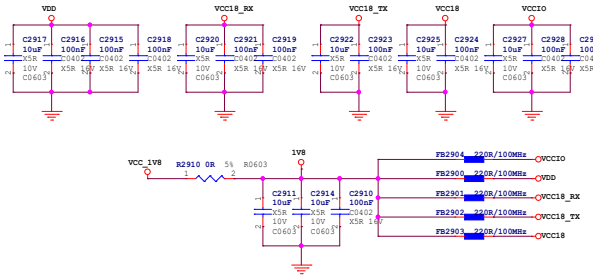
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	28.VO-LCM_MIPI_DSI_TX1		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	28 of 40

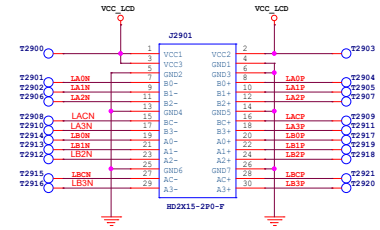
Single-eDP LCM

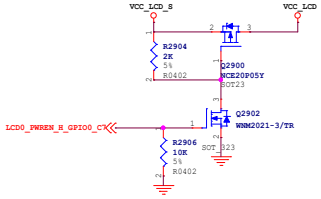


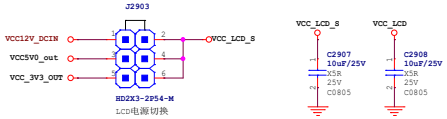
LT9211



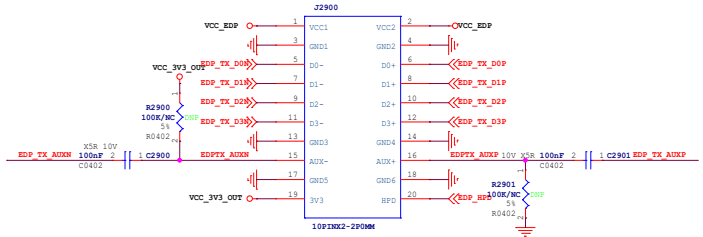


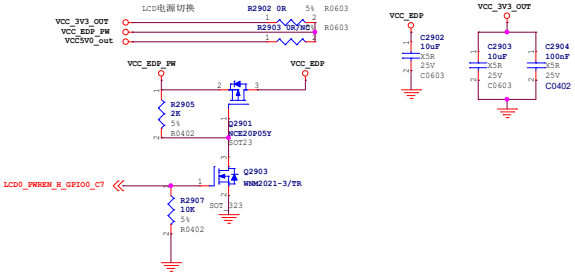


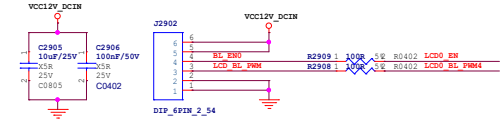




Note:
For EDP displays with edp1.2a or above, the bias resistors R5600 and R5601 of aux are not mounted.





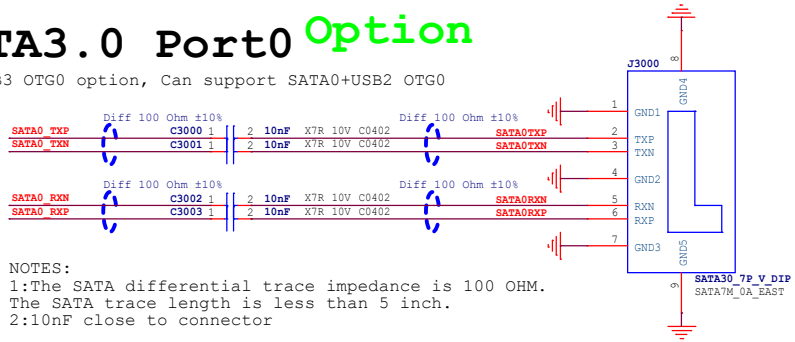


ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	29.VO-LCM_EDP/LVDS		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	29 of 40

SATA0_TXP
SATA0_TXN
SATA0_RXP
SATA0_RXN

SATA3.0 Port0 Option

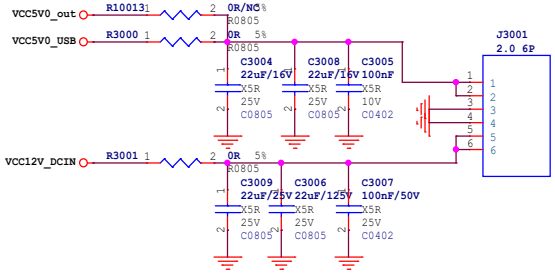
And USB3 OTG0 option, Can support SATA0+USB2 OTG0



NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA Power

The current is estimated according to the actual number of SATA
High power switching separate power supply is recommended for more than 2



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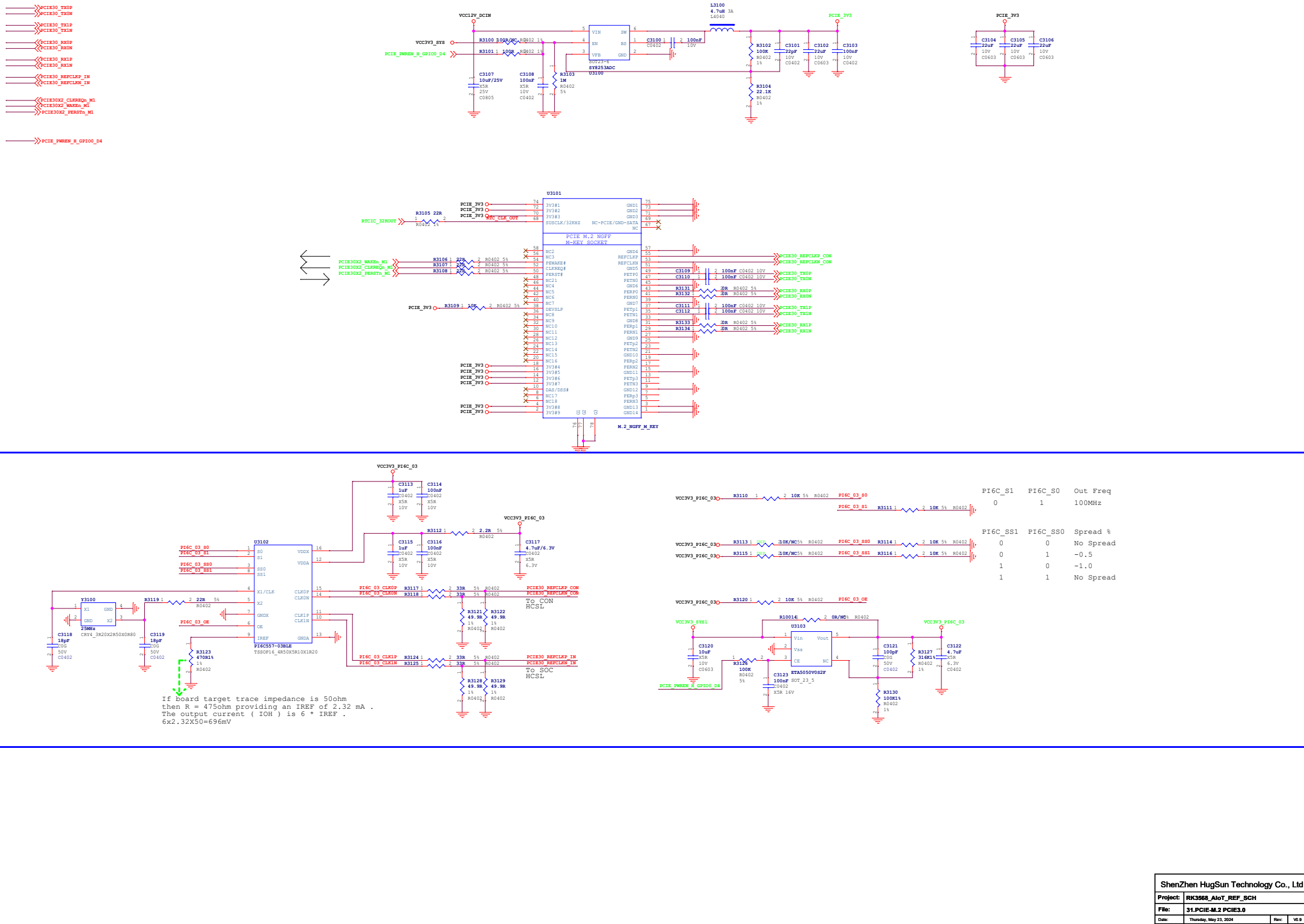
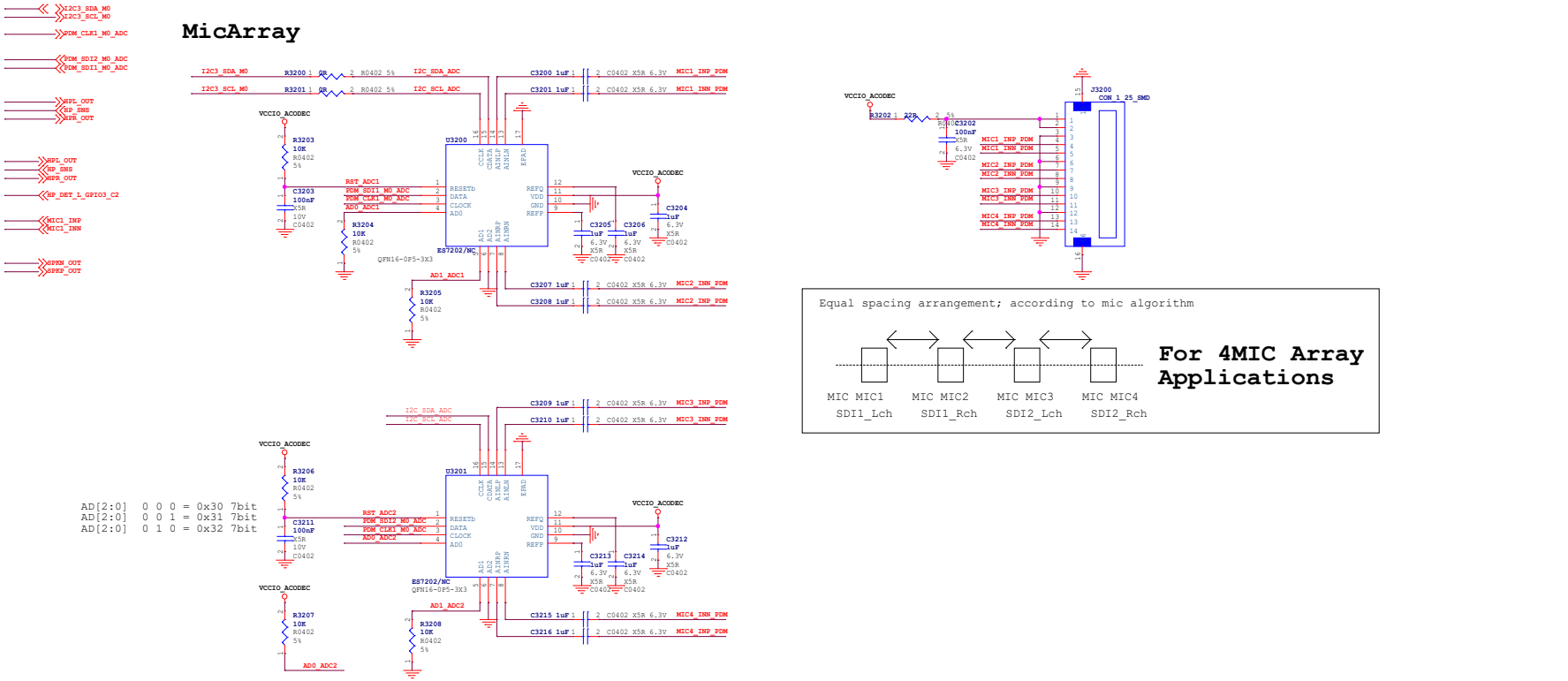
ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	30.SATA-SATA3.0 Slot_7P		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	30 of 40



ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	31.PCIE-M.2 PCIE3.0
Date:	Thursday, May 23, 2024
Rev:	V0.9
Designed by:	Wang
Sheet:	31 of 40

MicArray

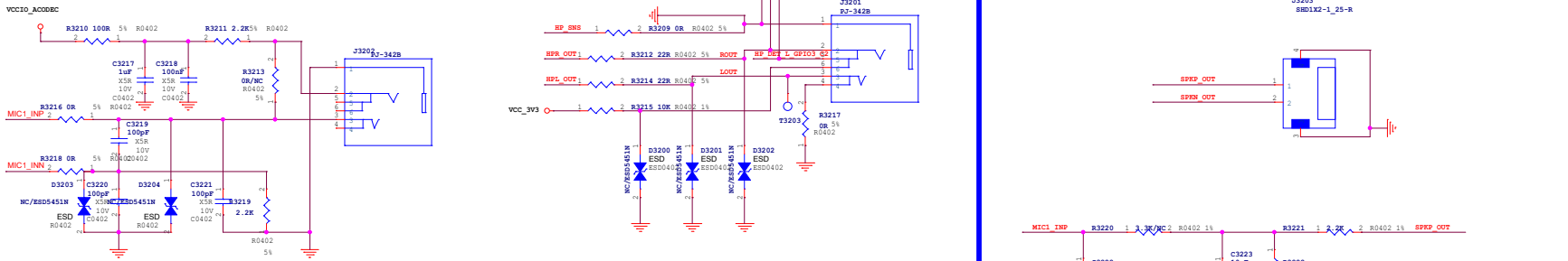


AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit
AD[2:0] 0 1 0 = 0x32 7bit

Equal spacing arrangement; according to mic algorithm

For 4MIC Array Applications

MIC0



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ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	32.Audio-MicArray_SPK
Date: Thursday, May 23, 2024	Rev: V0.9
Designed by: Wang	Sheet: 32 of 40

Working_LEDEN_H_GPIO0_B7

SARADC_VIN1_HW_ID

SARADC_VIN3_BOM_ID

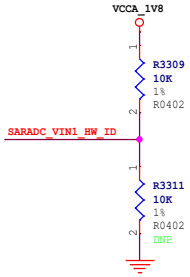
SATA0_ACT_LED

Work_LED

Power_LED

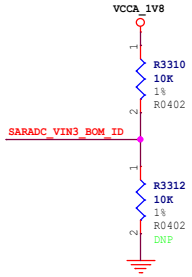
LED3

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

BOM_ID



SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

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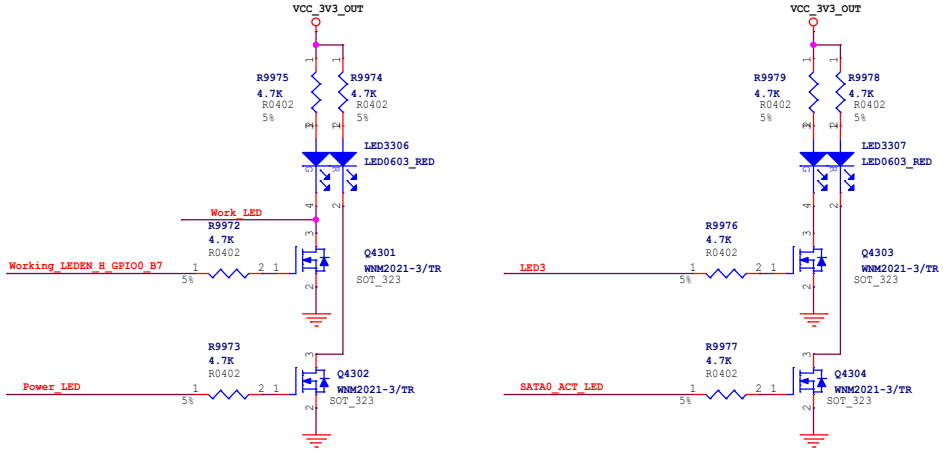
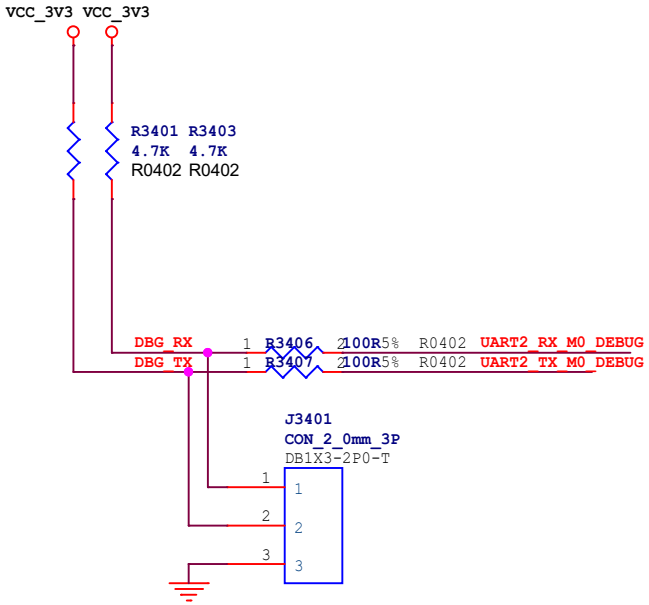


ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	33.LED/HW_ID/BOM_ID		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	33 of 40

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	34.Debug UART		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	34 of 40

Key Array

SARADC_VIN0_KEY/RECOVERY

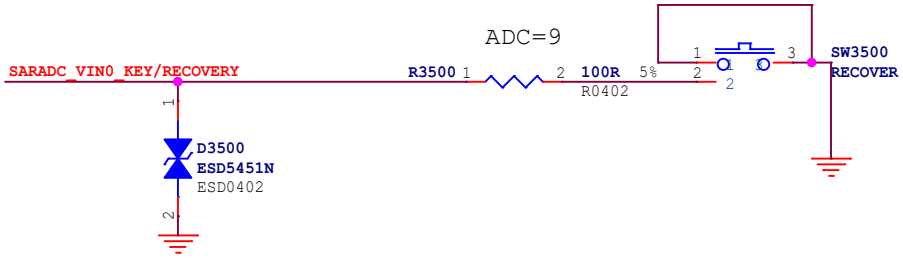
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

RESETn

RK809_PWRON

PWR_KEY_MCU

Work_LED

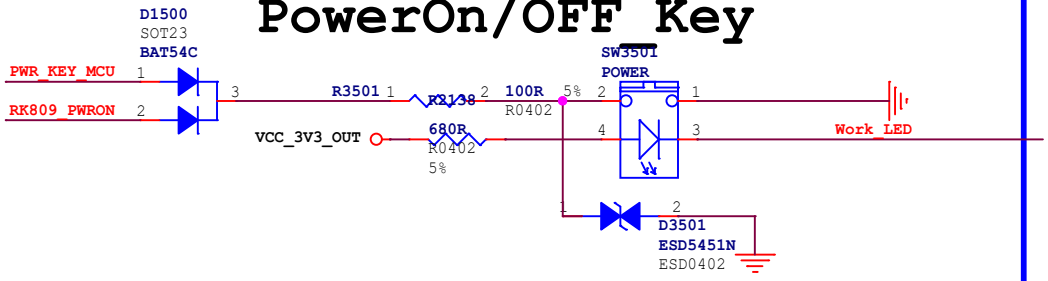


Note:

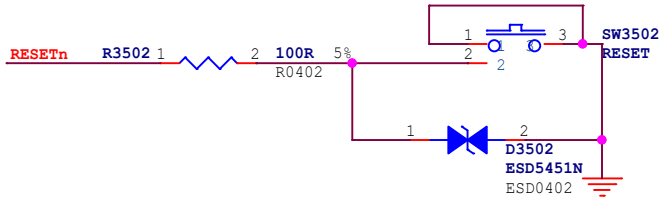
If there is no Key requirement,
It is suggested to reserve a
SW9200 Key to facilitate the
development debug

RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

PowerOn/OFF_Key

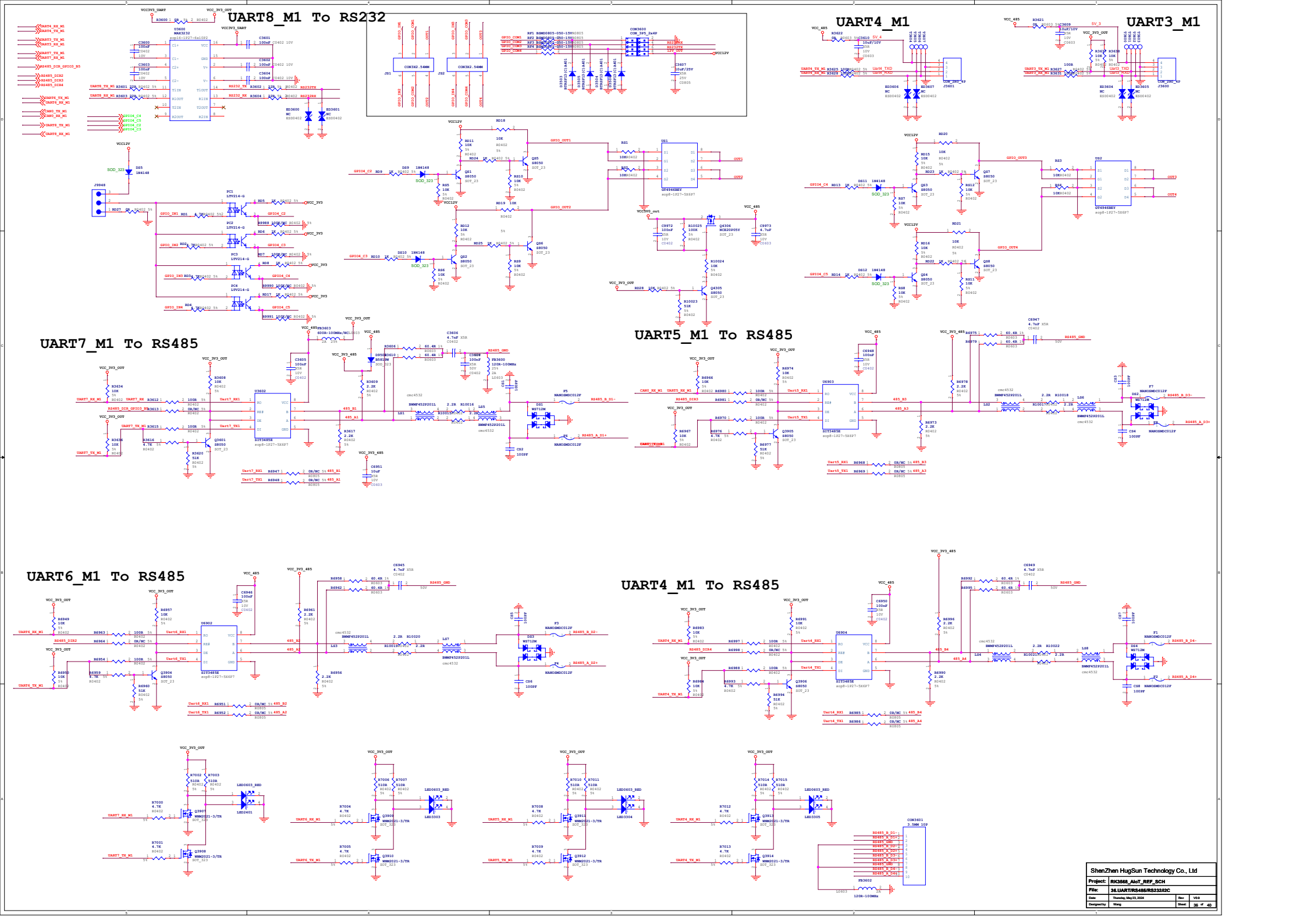


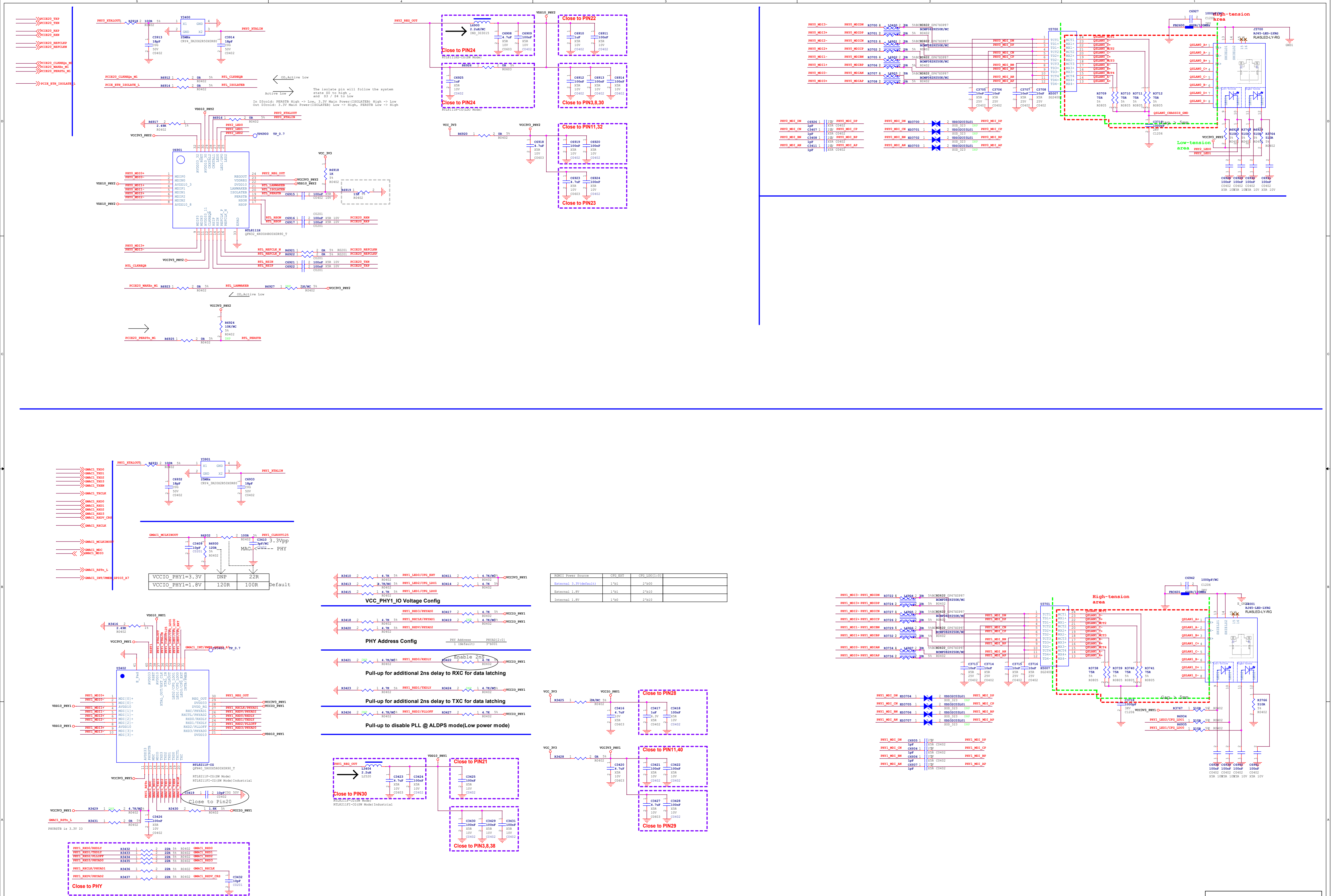
Reset_Key



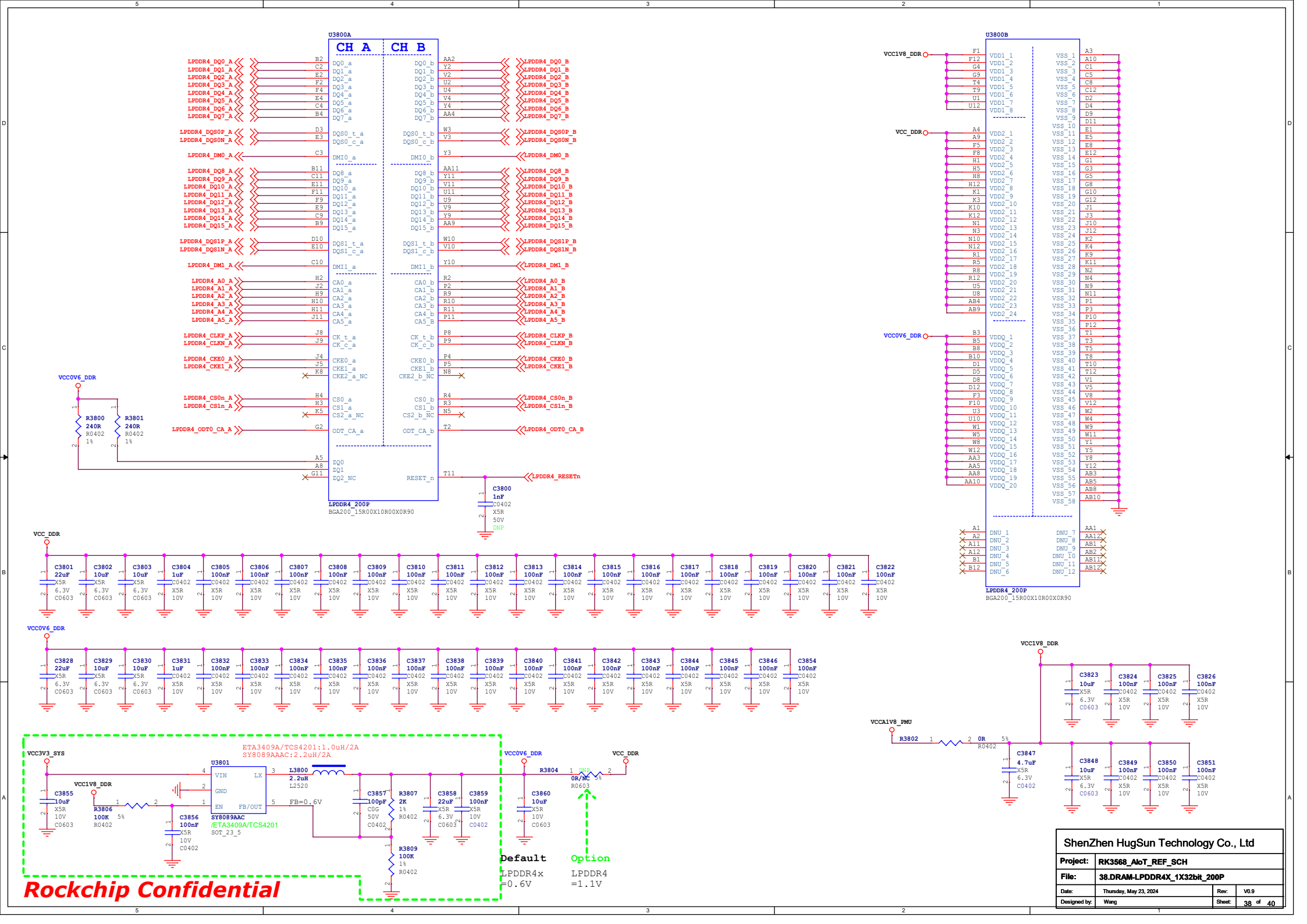
SARADC

ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	35.KEY Array/SARADC		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	35 of 40


UART8_M1 To RS232
UART4_M1
UART3_M1
UART7_M1 To RS485
UART5_M1 To RS485
UART6_M1 To RS485
UART4_M1 To RS485
ShenZhen HugSun Technology Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 36.UART/RS485/RS232/I2C
Date: Thursday, May 23, 2024
Rev: V0.9
Designed by: Wang
Sheet: 36 of 40



ShenZhen HugSun Technology Co., Ltd			
Project:	RK3568_AIoT_REF_SCH		
File:	37.Ethernet-GEPHY_RGMII_PCIE		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	37 of 40


U3800A
CH A
CH B
LPDDR4_DQ0_A
LPDDR4_DQ1_A
LPDDR4_DQ2_A
LPDDR4_DQ3_A
LPDDR4_DQ4_A
LPDDR4_DQ5_A
LPDDR4_DQ6_A
LPDDR4_DQ7_A
LPDDR4_DQS0P_A
LPDDR4_DQS0N_A
LPDDR4_DM0_A
LPDDR4_DQ8_A
LPDDR4_DQ9_A
LPDDR4_DQ10_A
LPDDR4_DQ11_A
LPDDR4_DQ12_A
LPDDR4_DQ13_A
LPDDR4_DQ14_A
LPDDR4_DQ15_A
LPDDR4_DQS1P_A
LPDDR4_DQS1N_A
LPDDR4_DM1_A
LPDDR4_A0_A
LPDDR4_A1_A
LPDDR4_A2_A
LPDDR4_A3_A
LPDDR4_A4_A
LPDDR4_A5_A
LPDDR4_CLKP_A
LPDDR4_CLKN_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_CS0n_A
LPDDR4_CS1n_A
LPDDR4_ODT0_CA_A
LPDDR4_200P
BGA200_15R00X10R00X0R90
LPDDR4_DQ0_B
LPDDR4_DQ1_B
LPDDR4_DQ2_B
LPDDR4_DQ3_B
LPDDR4_DQ4_B
LPDDR4_DQ5_B
LPDDR4_DQ6_B
LPDDR4_DQ7_B
LPDDR4_DQS0P_B
LPDDR4_DQS0N_B
LPDDR4_DM0_B
LPDDR4_DQ8_B
LPDDR4_DQ9_B
LPDDR4_DQ10_B
LPDDR4_DQ11_B
LPDDR4_DQ12_B
LPDDR4_DQ13_B
LPDDR4_DQ14_B
LPDDR4_DQ15_B
LPDDR4_DQS1P_B
LPDDR4_DQS1N_B
LPDDR4_DM1_B
LPDDR4_A0_B
LPDDR4_A1_B
LPDDR4_A2_B
LPDDR4_A3_B
LPDDR4_A4_B
LPDDR4_A5_B
LPDDR4_CLKP_B
LPDDR4_CLKN_B
LPDDR4_CKE0_B
LPDDR4_CKE1_B
LPDDR4_CS0n_B
LPDDR4_CS1n_B
LPDDR4_ODT0_CA_B
LPDDR4_RESETn
VCC0V6_DDR
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 1nF C0402 X5R 50V DNP
U3800B
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC_DDR
C3801 22uF X5R 6.3V C0603
C3802 10uF X5R 6.3V C0603
C3803 10uF X5R 6.3V C0603
C3804 1uF C0402 X5R 10V
C3805 100nF C0402 X5R 10V
C3806 100nF C0402 X5R 10V
C3807 100nF C0402 X5R 10V
C3808 100nF C0402 X5R 10V
C3809 100nF C0402 X5R 10V
C3810 100nF C0402 X5R 10V
C3811 100nF C0402 X5R 10V
C3812 100nF C0402 X5R 10V
C3813 100nF C0402 X5R 10V
C3814 100nF C0402 X5R 10V
C3815 100nF C0402 X5R 10V
C3816 100nF C0402 X5R 10V
C3817 100nF C0402 X5R 10V
C3818 100nF C0402 X5R 10V
C3819 100nF C0402 X5R 10V
C3820 100nF C0402 X5R 10V
C3821 100nF C0402 X5R 10V
C3822 100nF C0402 X5R 10V
VCC0V6_DDR
C3828 22uF X5R 6.3V C0603
C3829 10uF X5R 6.3V C0603
C3830 10uF X5R 6.3V C0603
C3831 1uF C0402 X5R 10V
C3832 100nF C0402 X5R 10V
C3833 100nF C0402 X5R 10V
C3834 100nF C0402 X5R 10V
C3835 100nF C0402 X5R 10V
C3836 100nF C0402 X5R 10V
C3837 100nF C0402 X5R 10V
C3838 100nF C0402 X5R 10V
C3839 100nF C0402 X5R 10V
C3840 100nF C0402 X5R 10V
C3841 100nF C0402 X5R 10V
C3842 100nF C0402 X5R 10V
C3843 100nF C0402 X5R 10V
C3844 100nF C0402 X5R 10V
C3845 100nF C0402 X5R 10V
C3846 100nF C0402 X5R 10V
C3854 100nF C0402 X5R 10V
VCC1V8_DDR
C3823 10uF X5R 6.3V C0603
C3824 100nF C0402 X5R 10V
C3825 100nF C0402 X5R 10V
C3826 100nF C0402 X5R 10V
VCCA1V8_PMU
R3802 0R R0402 5%
C3847 4.7uF X5R 6.3V C0402
C3848 10uF X5R 6.3V C0603
C3849 100nF C0402 X5R 10V
C3850 100nF C0402 X5R 10V
C3851 100nF C0402 X5R 10V
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
VCC3V3_SYS
VCC1V8_DDR
U3801
VIN
LX
GND
EN
FB/OUT
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
L3800 2.2uH L2520
FB=0.6V
C3855 10uF X5R 10V C0603
R3806 100K R0402 5%
C3856 100nF X5R 10V C0402
C3857 100pF C0G 50V C0402
R3807 2K 1% R0402
C3858 22uF X5R 6.3V C0603
C3859 100nF X5R 10V C0402
R3809 100K 1% R0402
VCC0V6_DDR
R3804 0R/NC R0603 5%
C3860 10uF X5R 10V C0603
VCC_DDR
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
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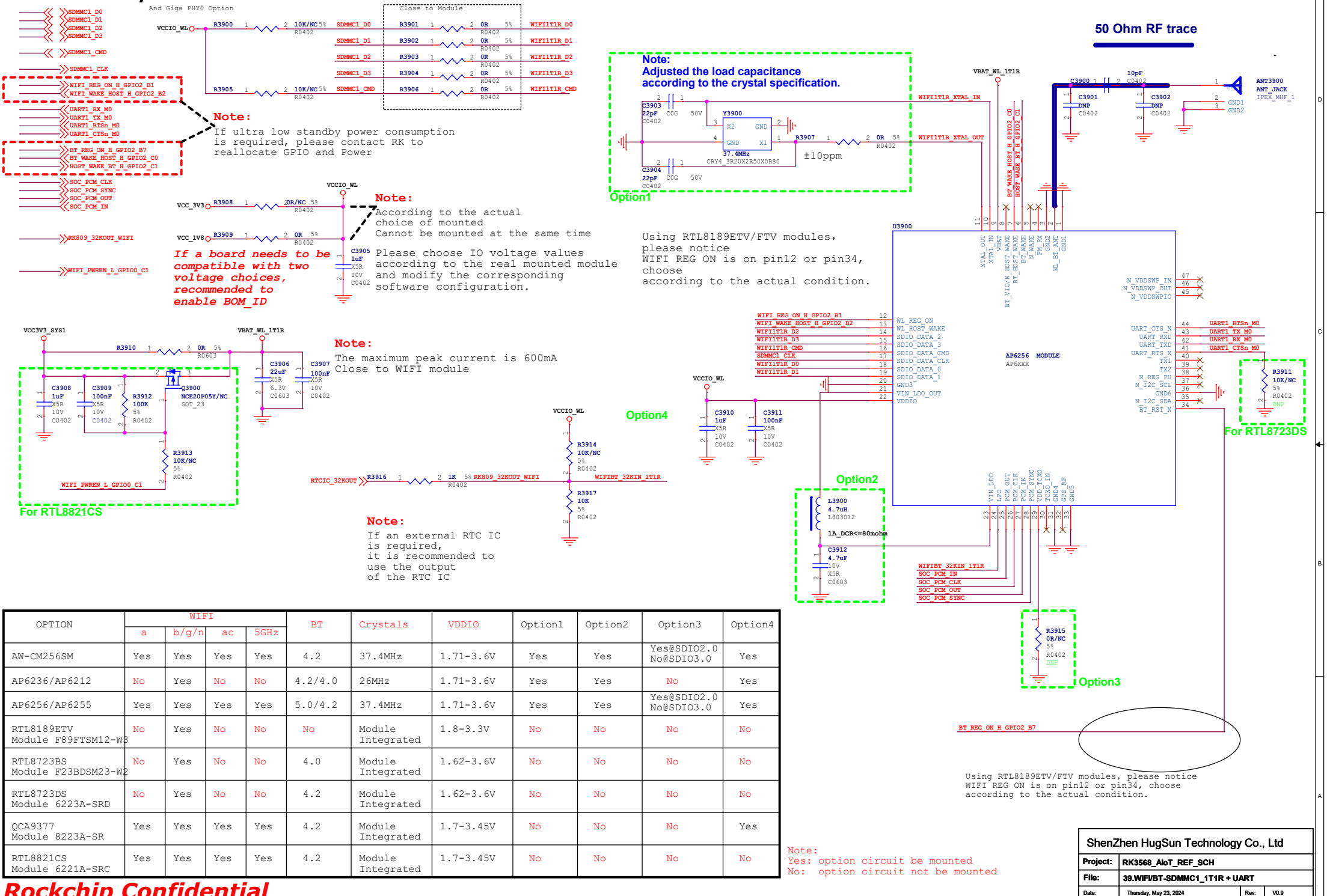
ShenZhen HugSun Technology Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 38.DRAM-LPDDR4X_1X32bit_200P
Date: Thursday, May 23, 2024
Rev: V0.9
Designed by: Wang
Sheet: 38 of 40

SDIO WIFI/BT MODULE



OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

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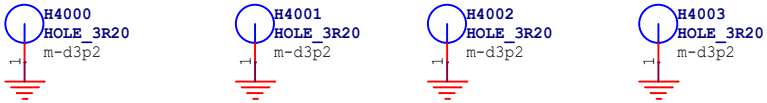
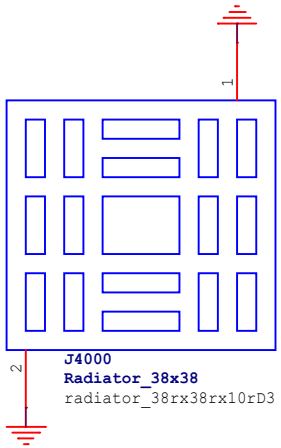
ShenZhen HugSun Technology Co., Ltd	
Project:	RK3568_AIoT_REF_SCH
File:	39.WIFI/BT-SDMMC1_1T1R + UART
Date: Thursday, May 23, 2024	Rev: V0.9
Designed by: Wang	Sheet: 39 of 40





TOP Mark

BOTTOM Mark

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ShenZhen HugSun Technology Co., Ltd			
Project:	**RK3568_AIoT_REF_SCH**		
File:	**40.Mark/Hole/Heatsink**		
Date:	Thursday, May 23, 2024	Rev:	V0.9
Designed by:	Wang	Sheet:	40 of 40