Schematics For RK3566 BOX

RK3566_BOX_Demo1_DDR4P408DD4_V10

Main Functions Introduction

1) PMIC: DiscretePower(DCIN 12V)
2) RAM: DDR4 4x8Bit
3) ROM: eMMC,Nand Flash(Option)
4) Support: 1 x Micro SD Card3.0
5) Support: 1 x SATA3.0 Connector (7pin)
6) Support: 1 x USB2.0 OTG + 1 x USB3.0 HOST + 2 x USB2.0 HOST
7) Support: 1 x HDMI2.0 TX
8) Support: 1 x Optical S/PDIF TX
9) Support: 1 x 4Lane MIPI CSI RX
10) Support: 1 x 10/100/1000 Ethernet(RGMII)
11) Support: 1 x a/b/g/n/ac Wi-Fi + BT 5.0(2T2R)
12) Support: 1 x IR Receiver
13) Support: 1 x Recovery Key
14) Support: 1 x Power LED,1 x Working LED,1 x IR LED,1 x SATA ACT LED
15) Support: Debug UART

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	00.Cover Page				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	1 of 35

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	01.Index and Notes				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
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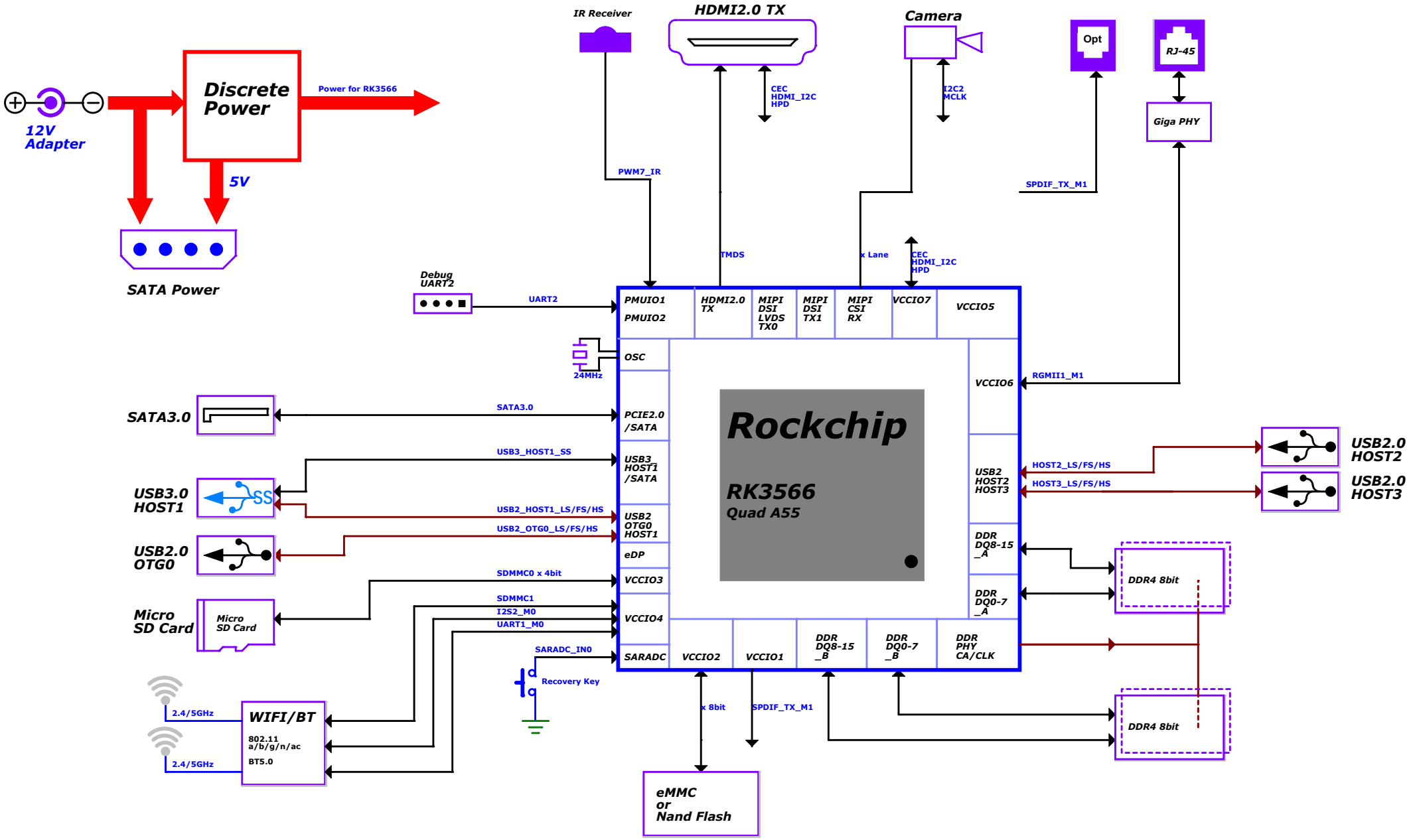
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-01-05	Zhangdz	1:Revision preliminary version	

RK3566 Ref Block Diagram



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	03.Block Diagram
Date:	Wednesday, March 24, 2021
Rev:	V1.0
Designed by:	Zhangtz
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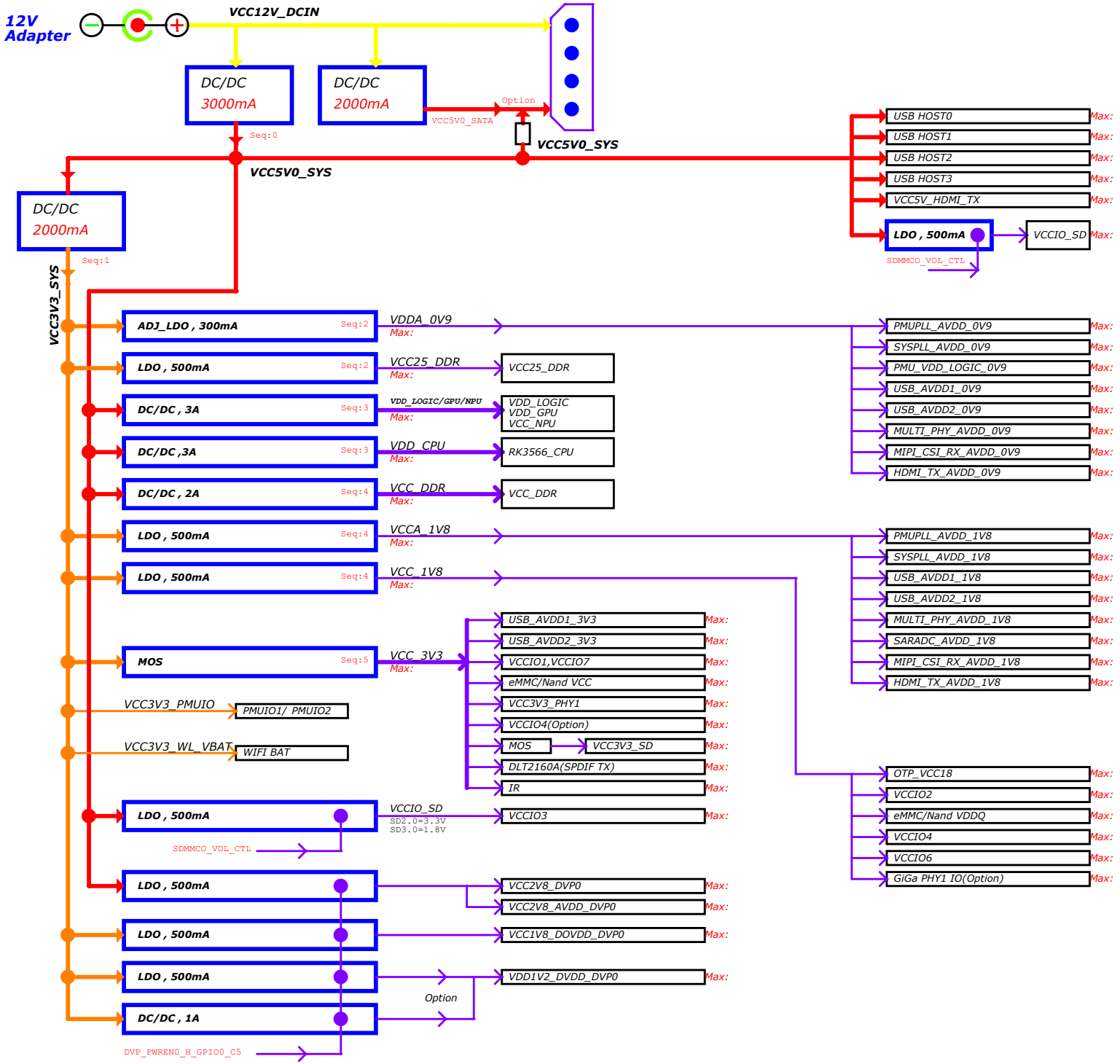
Power Diagram



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	04.Power Diagram
Date:	Wednesday, March 24, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
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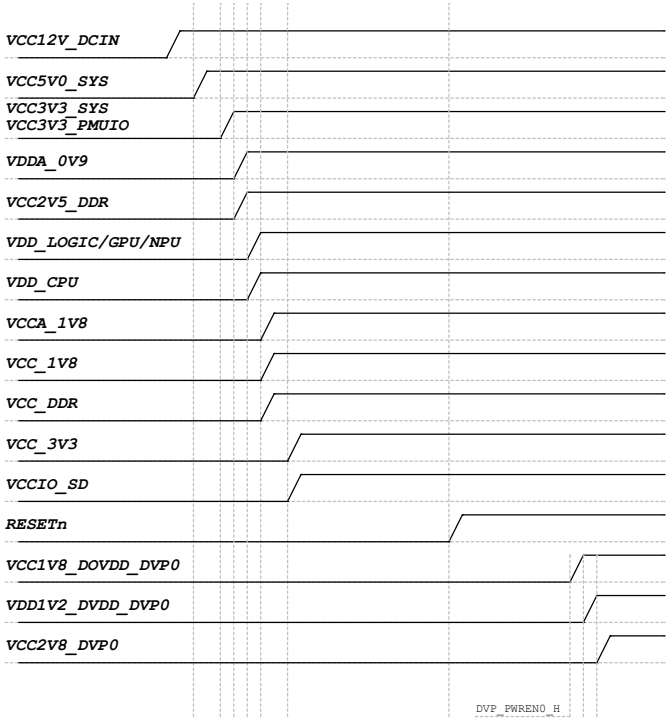
Power Sequence



Power Supply	Channel	Supply Limit	Power Name	Time Slot	Default Voltage
VCC12V_DCIN	BUCK	3.0A	VCC5V0_SYS	Slot:0	3.3V
VCC12V_DCIN	BUCK	3.0A	VCC3V3_SYS	Slot:1	5.2V
VCC3V3_SYS			VCC3V3_PMUIO	Slot:1	3.3V
VCC3V3_SYS	LDO	0.3A	VDDA_0V9	Slot:2	0.9V
VCC3V3_SYS	LDO	0.3A	VCC2V5_DDR	Slot:2	2.5V
VCC5V0_SYS	BUCK	3.0A	VDD_LOGIC/GPU/NPU	Slot:3	0.9V
VCC5V0_SYS	BUCK	5.0A	VDD_CPU	Slot:3	0.9V
VCC3V3_SYS	LDO	0.5A	VCC_1V8	Slot:4	1.8V
VCC3V3_SYS	LDO	0.5A	VCCA_1V8	Slot:4	1.8V
VCC5V0_SYS	BUCK	1.5A	VCC_DDR	Slot:4	1.2V DDR4
VCC3V3_SYS	MOS	2A	VCC_3V3	Slot:5	3.3V
VCC5V0_SYS	LDO	0.5A	VCCIO_SD	Slot:5A	3.3V
VCC3V3_PMUIO	RESETn				
VCC3V3_SYS	LDO	0.5A	VCC1V8_DOVDD_DVP0		1.8V
VCC3V3_SYS	LDO or BUCK	0.5A/1A	VDD1V2_DVDD_DVP0		1.2V
VCC5V0_SYS	LDO	0.5A	VCC2V8_DVP0		2.8V

IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMUIO	VCC3V3_SYS	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMUIO	VCC3V3_SYS	3.3V	
VCCIO1	Pin H17	✓	✓	VCC_3V3	VCC_3V3	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	SD2.0=3.3V-->SD3.0=1.8V
VCCIO4	Pin J21	✓	✓	VCCIO_WL	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓				
VCCIO6	Pin R9 Pin U9	✓	✓	VCC_1V8	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCC_3V3	VCC_3V3	3.3V	

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Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	05.Power Sequence/IO Domain Map				
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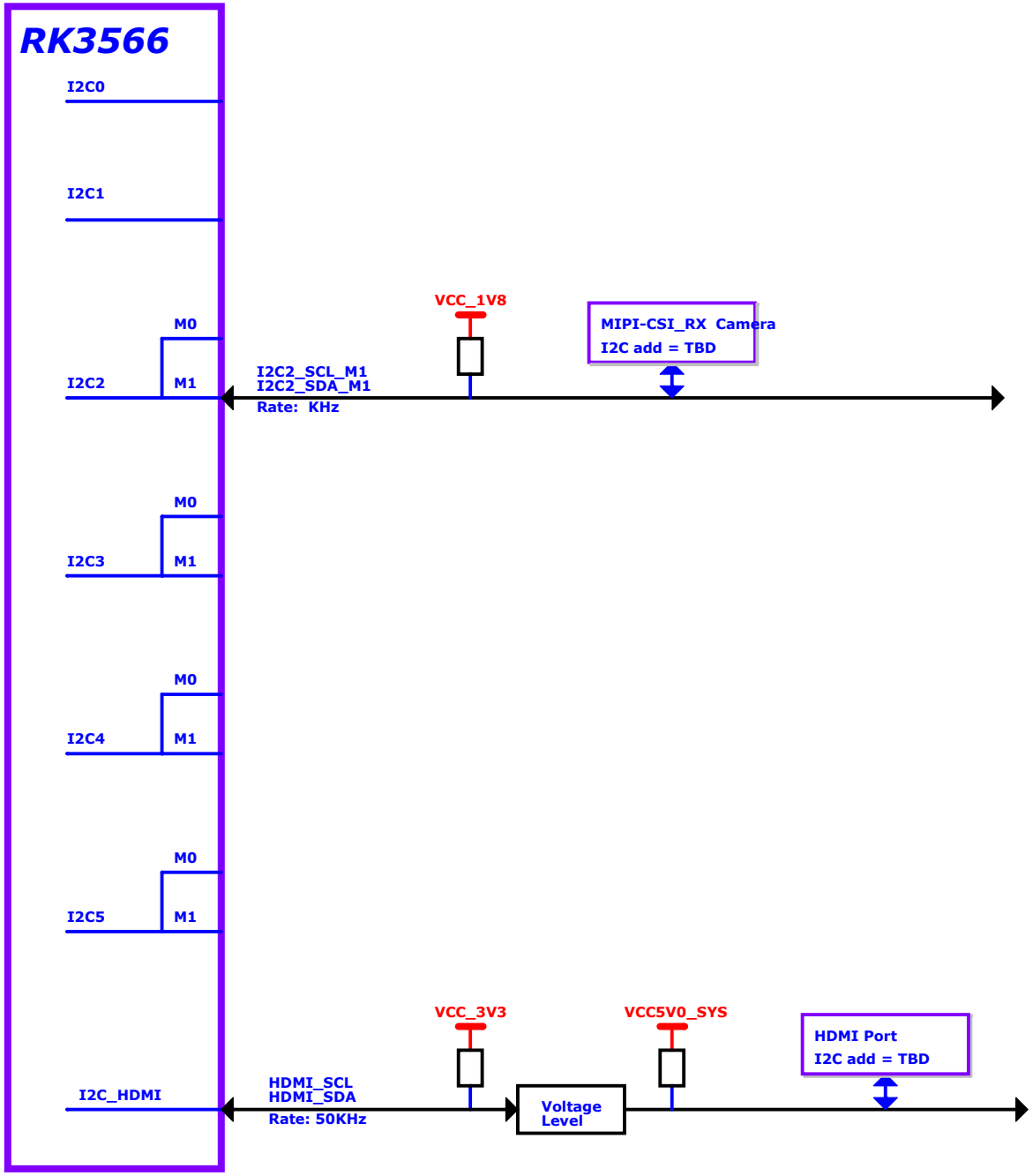
I2C MAP



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	07.I2C Bus Map				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
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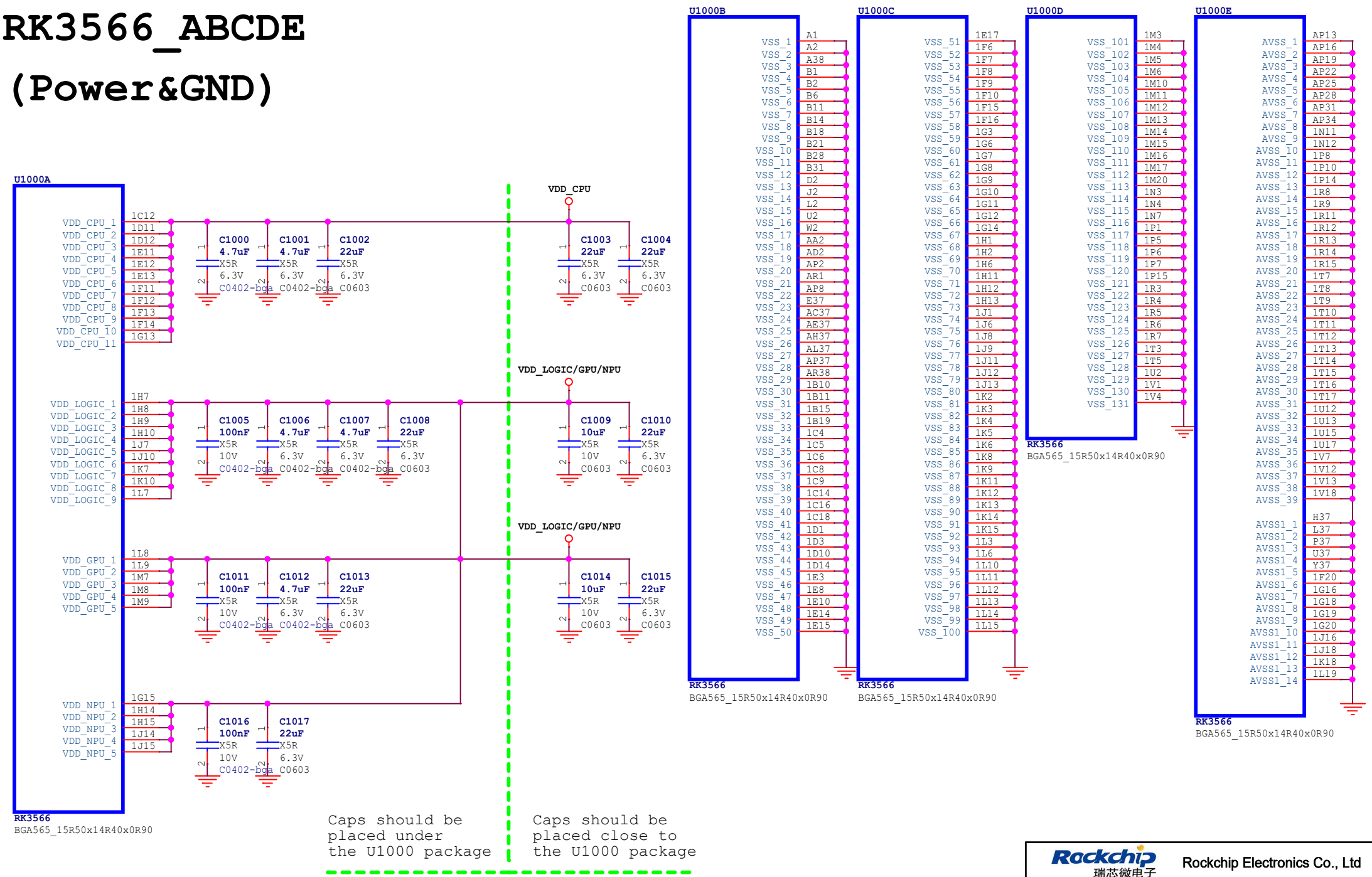
RK3566_ABCDE

(Power&GND)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	10.RK3566_Power/GND				
Date:	Monday, July 12, 2021			Rev:	V1.0
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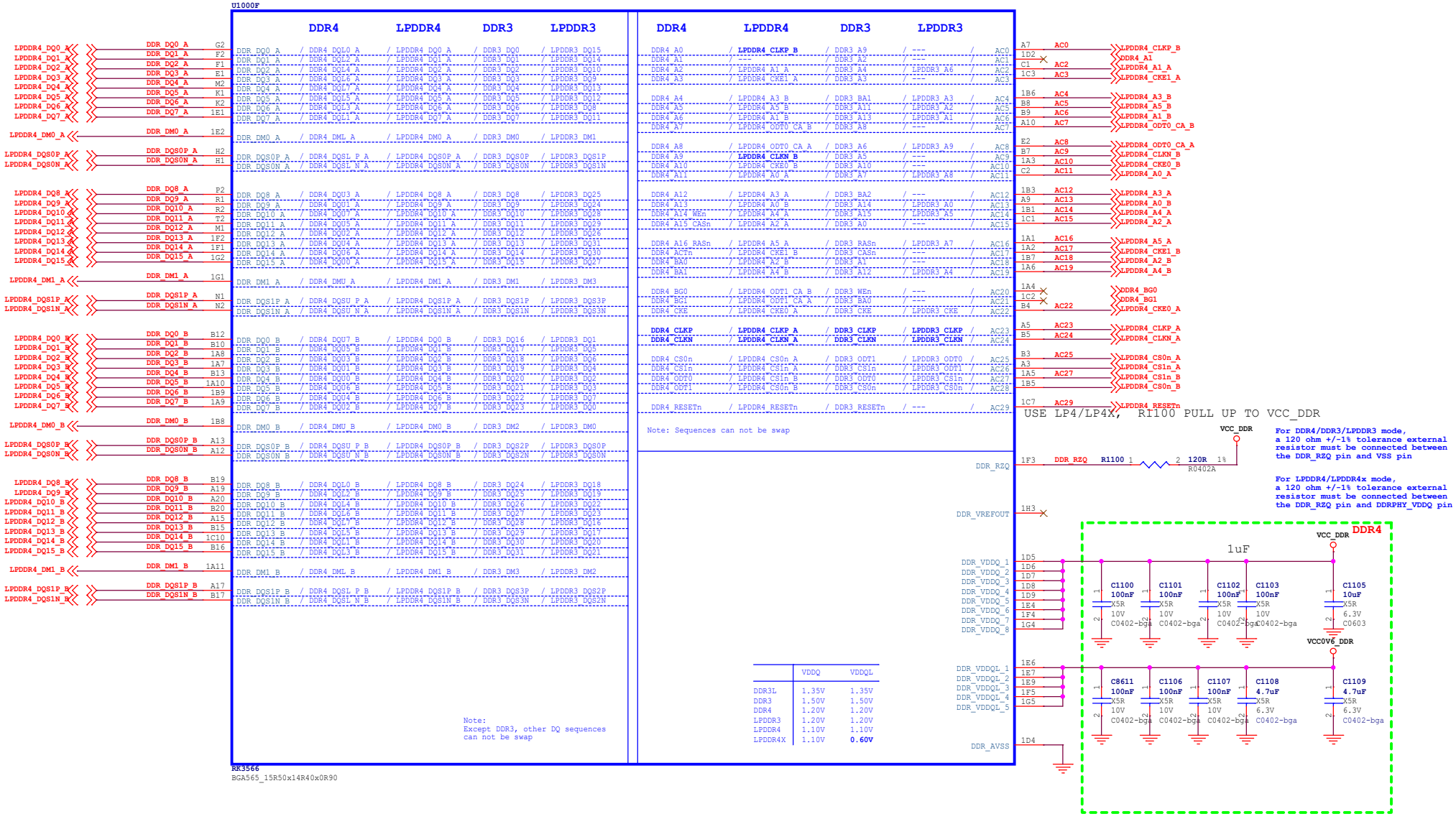
RK3566_F(DDR PHY)



	VDDQ	VDDQL
DDR3L	1.35V	1.35V
DDR3	1.50V	1.50V
DDR4	1.20V	1.20V
LPDDR3	1.20V	1.20V
LPDDR4	1.10V	1.10V
LPDDR4X	1.10V	**0.60V**

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Project:	RK3566_BOX_Demo1_DDR4P408DD4	
File:	11.RK3566_DDR PHY	
Date:	Monday, July 12, 2021	Rev: V1.0
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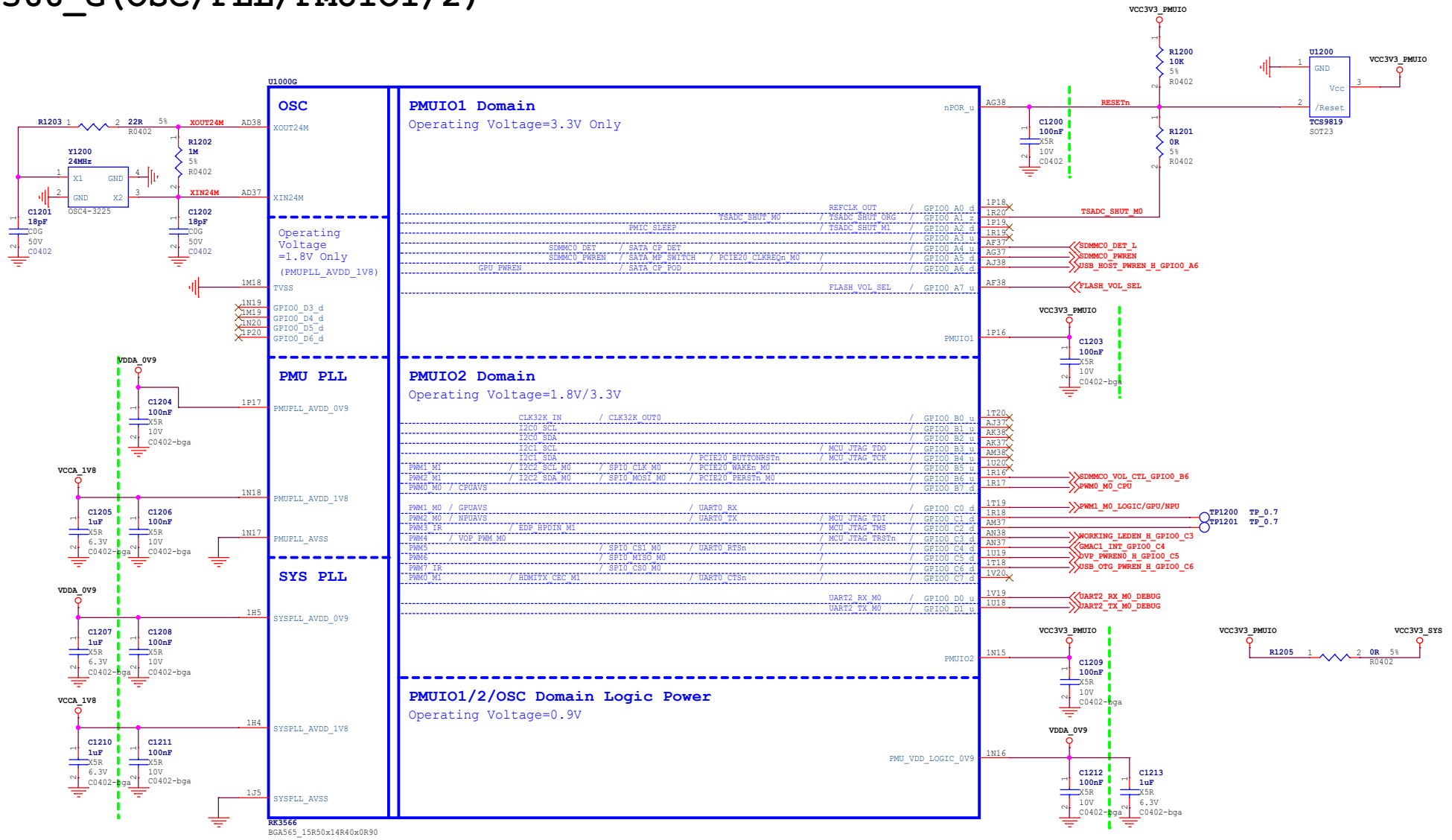
RK3566_G(OSC/PLL/PMUIO1/2)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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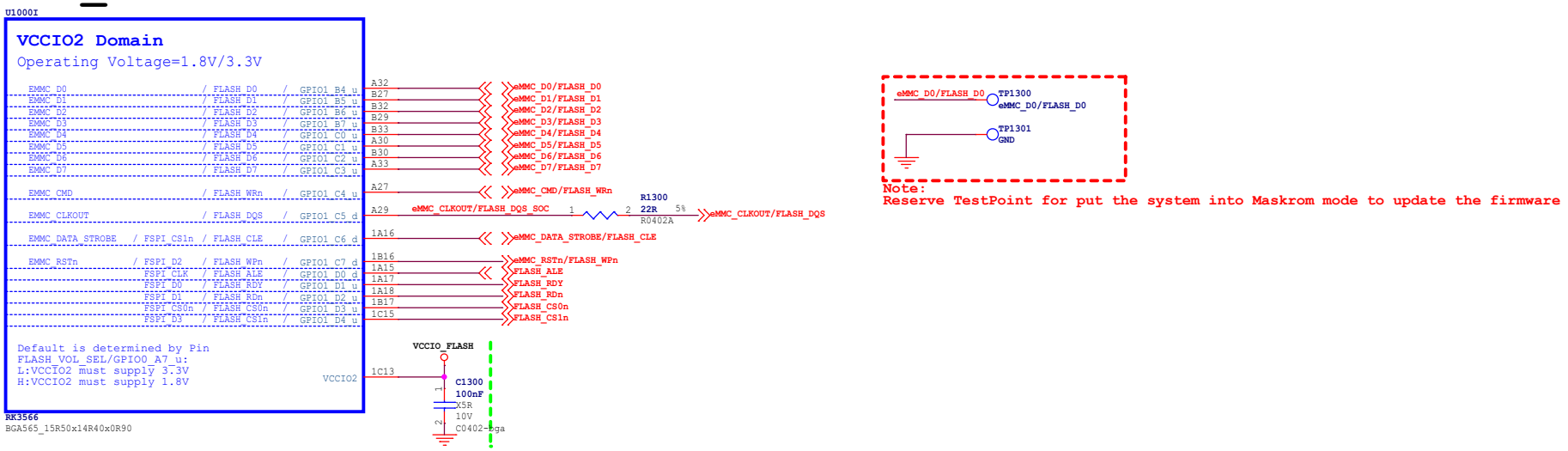
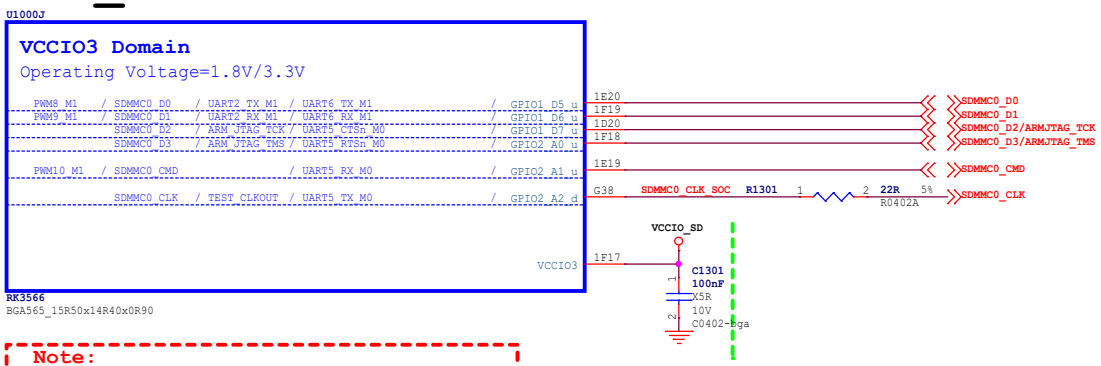
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	12.RK3566_OSC/PLL/PMUIO				
Date:	Tuesday, July 13, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	10 of 35

RK3566_I(VCCIO2 Domain)



RK3566_J(VCCIO3 Domain)



Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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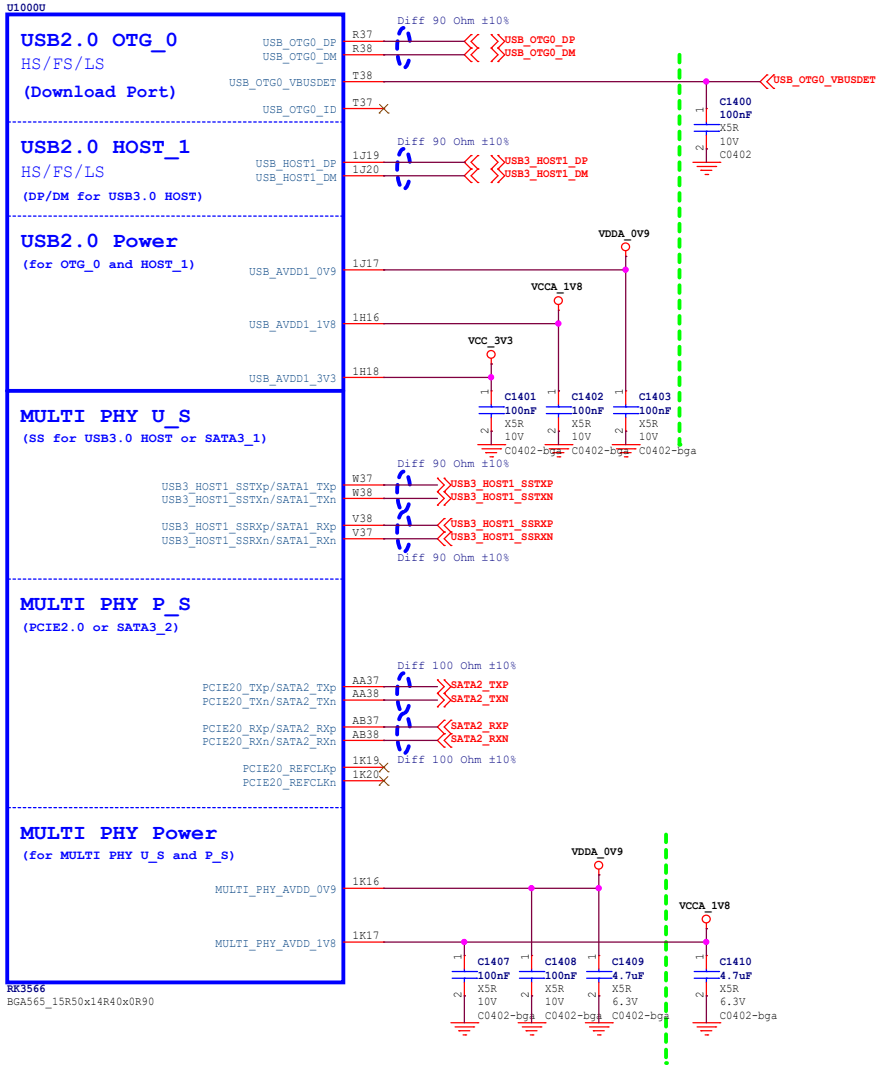
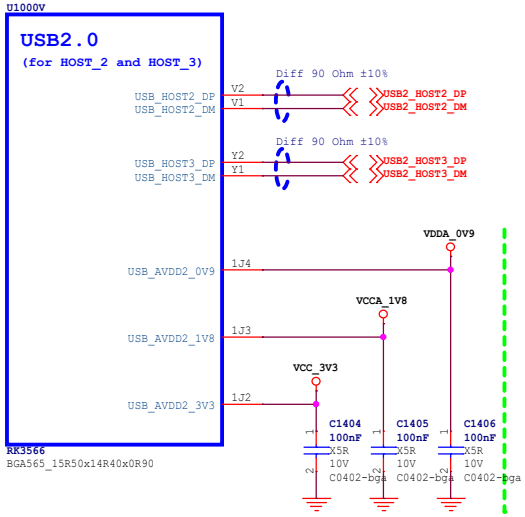
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	13.RK3566_Flash/SD Controller				
Date:	Monday, July 12, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	11 of 35

RK3566_U(USB3.0/PCIe2.0 x1)



RK3566_V(USB2.0 HOST)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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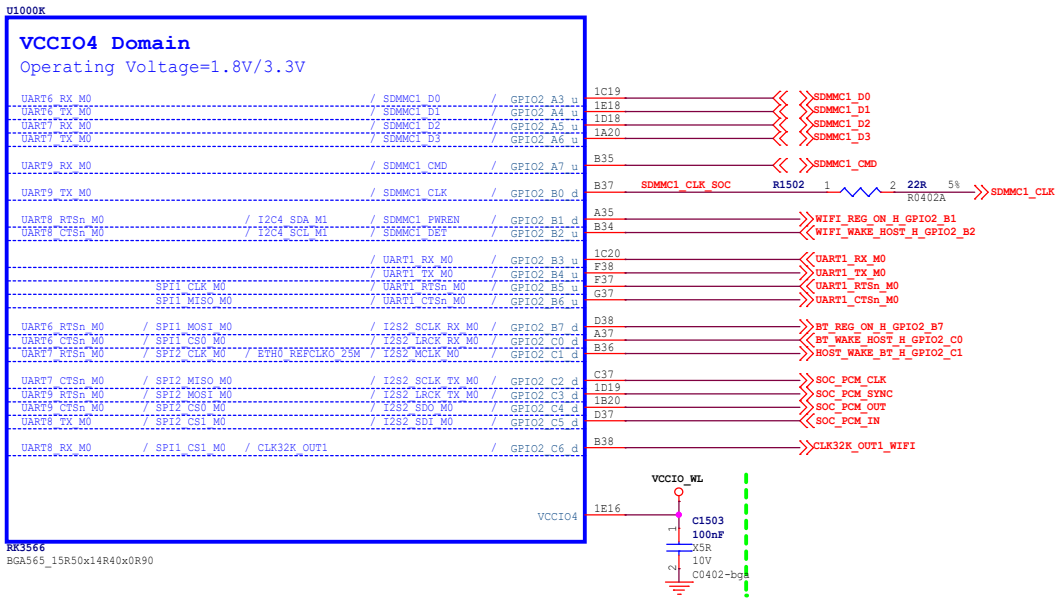
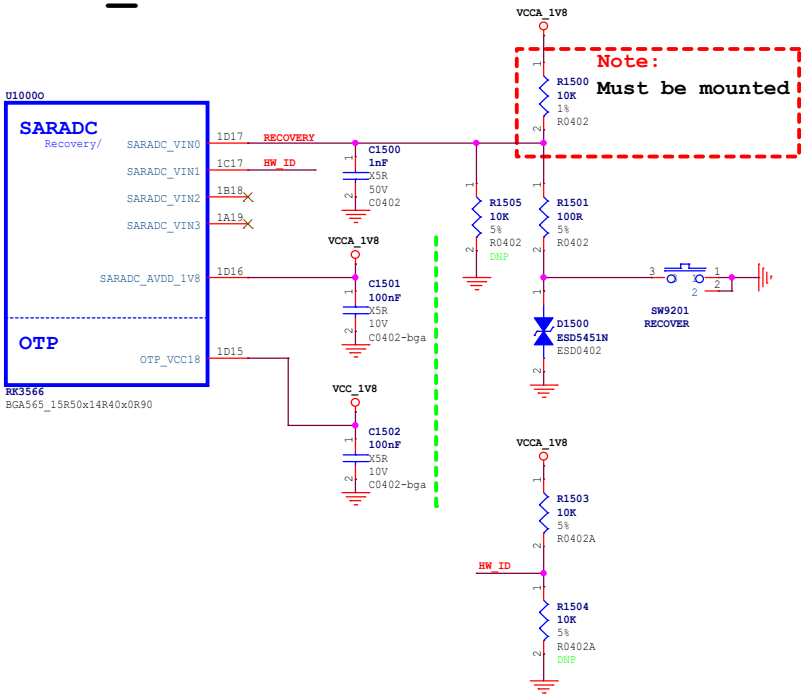
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	14.RK3566_USB/PCIe PHY				
Date:	Tuesday, July 13, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	12 of 35

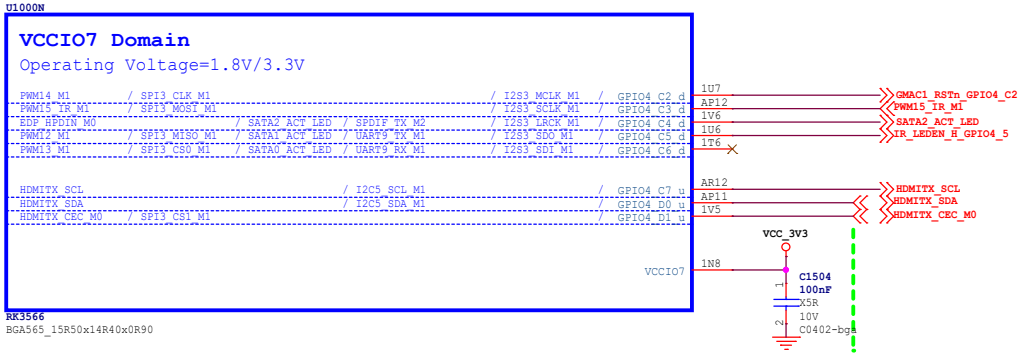
RK3566_K(VCCIO4 Domain)



RK3566_O(SARADC/OTP)



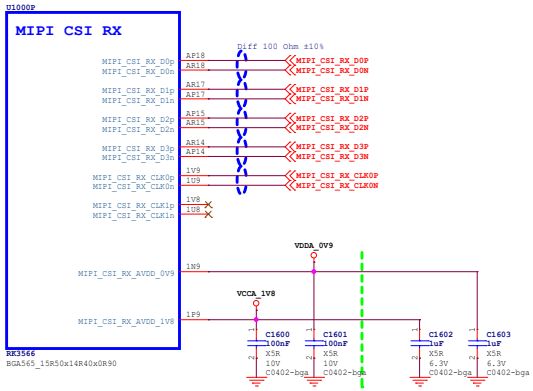
RK3566_N(VCCIO7 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

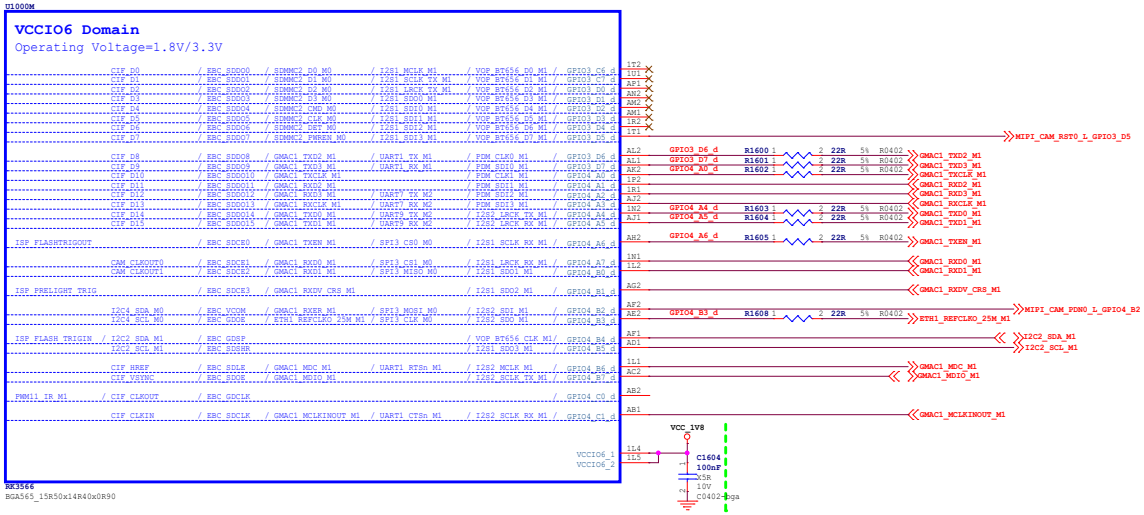
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	15.RK3566_SARADC/GPIO				
Date:	Monday, July 12, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	13 of 35

RK3566_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3566_M(VCCIO6 Domain)



Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	16.RK3566_VI Interface
Date:	Monday, July 12, 2021
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Designed by:	Zhangtz
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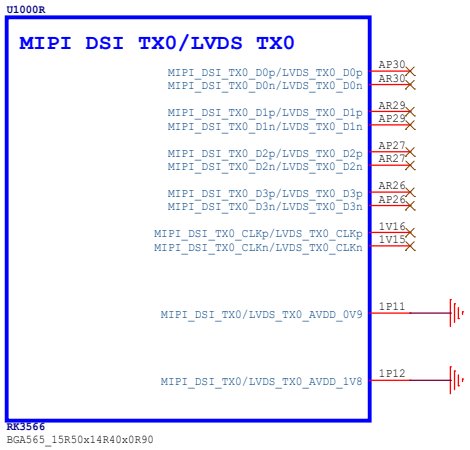
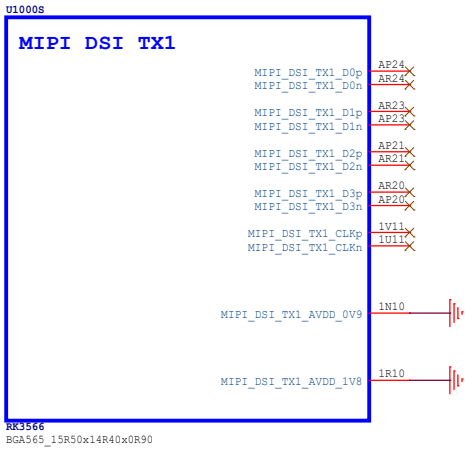
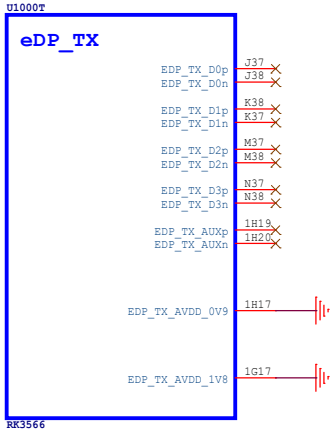
RK3566_R(MIPI_DSI_TX0/LVDS_TX0)



RK3566_S(MIPI_DSI_TX1)



RK3566_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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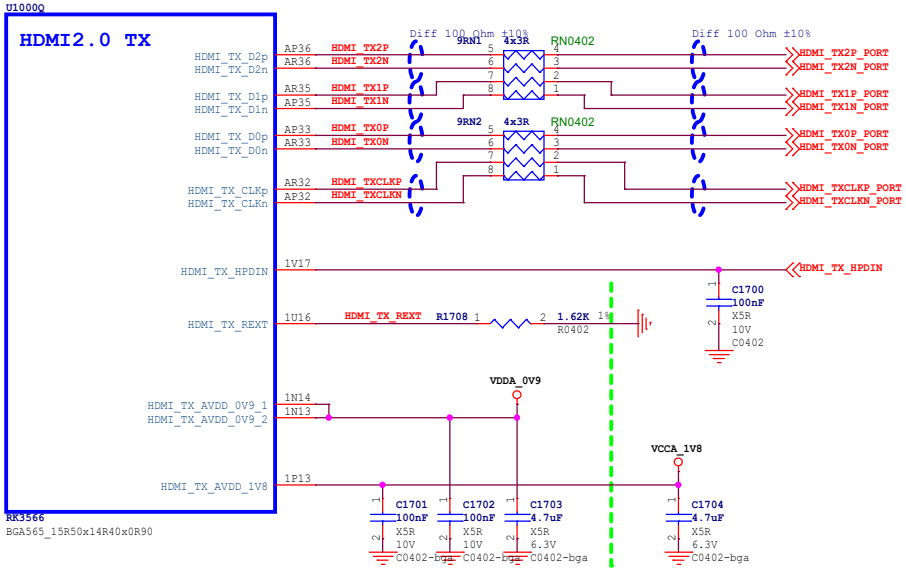
RK3566_Q(HDMI2.0 TX)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	17.RK3566_VO Interface_1				
Date:	Monday, July 12, 2021			Rev:	V1.0
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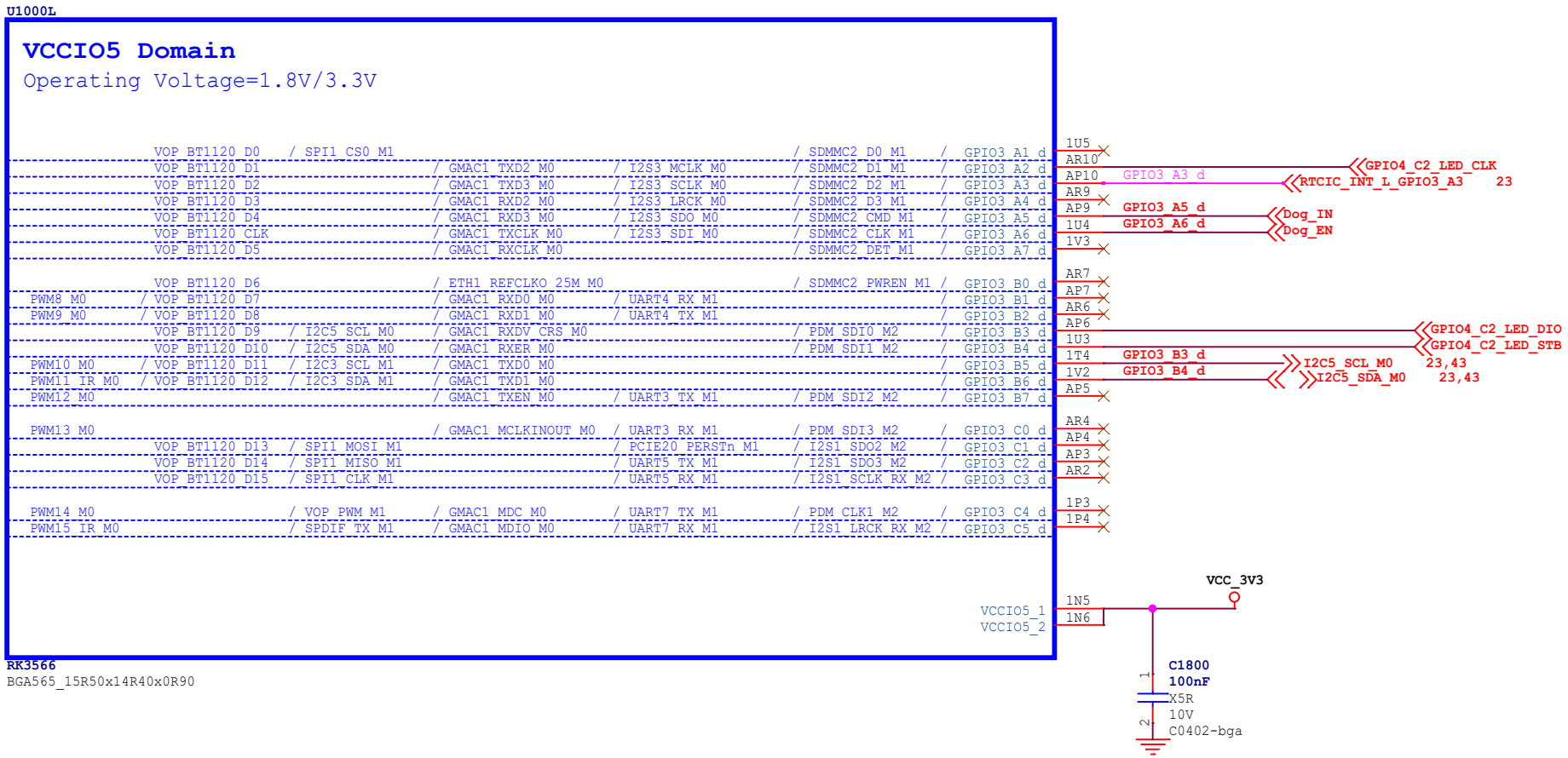
RK3566_L(VCCIO5 Domain)

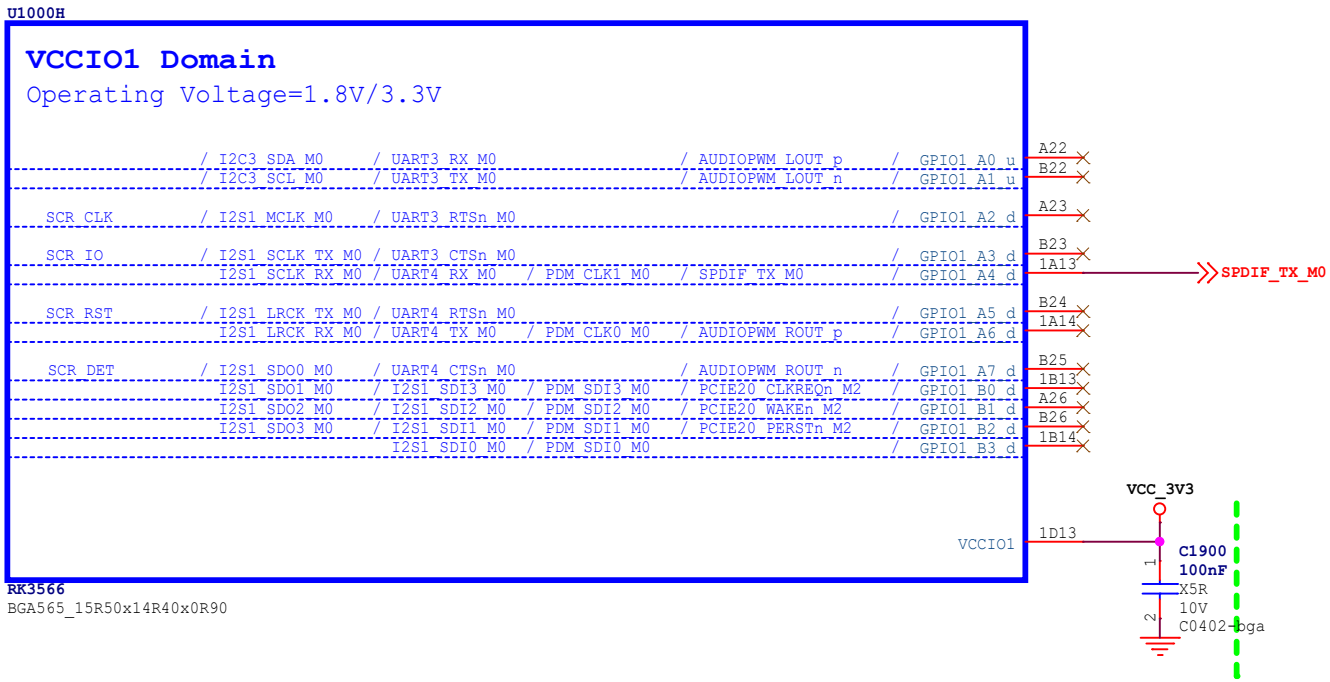


Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	18.RK3566_VO Interface_2				
Date:	Monday, July 12, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	16 of 35

RK3566_H(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	19.RK3566_Audio Interface				
Date:	Monday, July 12, 2021			Rev:	V1.0
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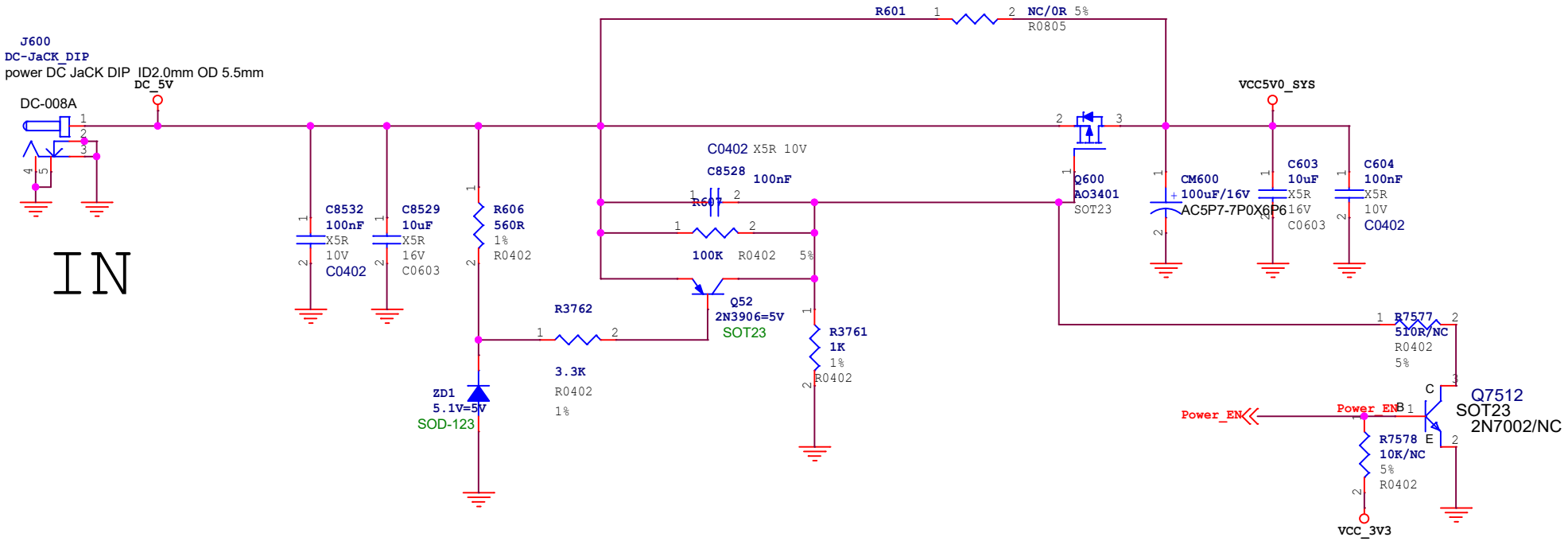
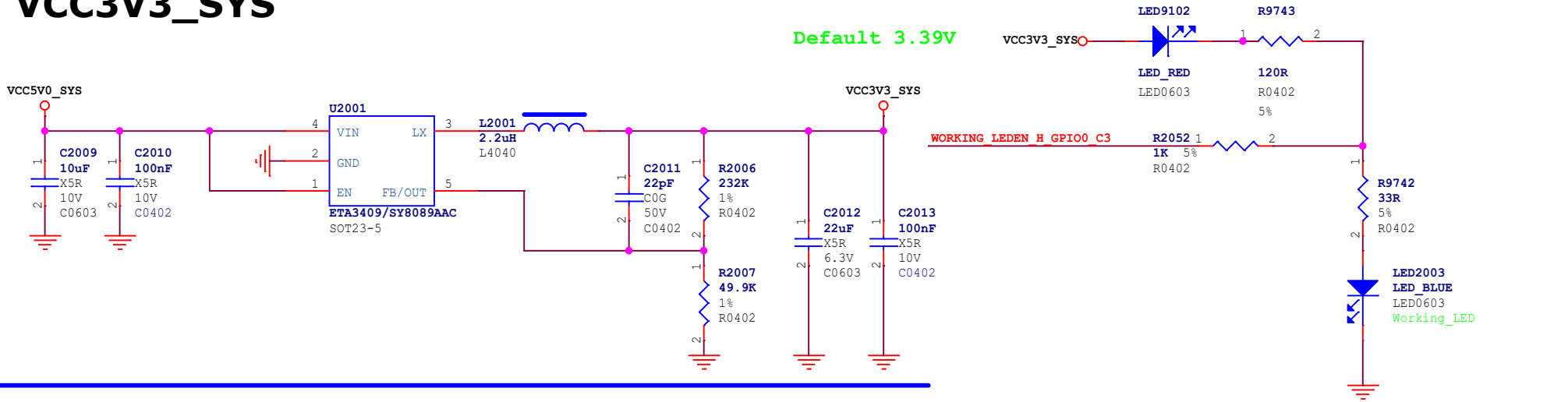
DC IN



VCC3V3_SYS



设备正常运行时呈蓝色常亮状态；
设备待机时呈呼吸灯状态。

WORKING_LEDEN_H_GPIO0_C3

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	20.Power_DC IN 5V				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
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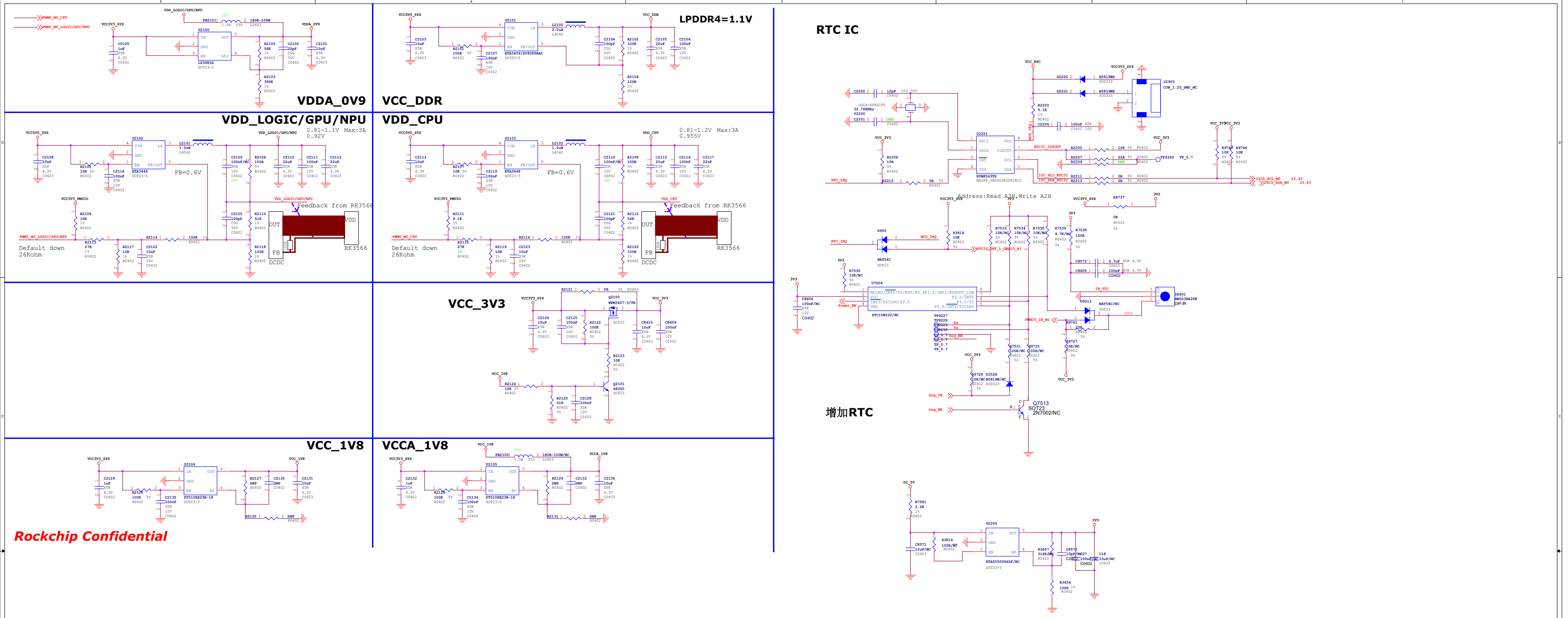

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	21.Power_DiscretePower RTC
Date:	Friday, July 16, 2021
Rev:	V1.0
Designed by:	Zhangdz
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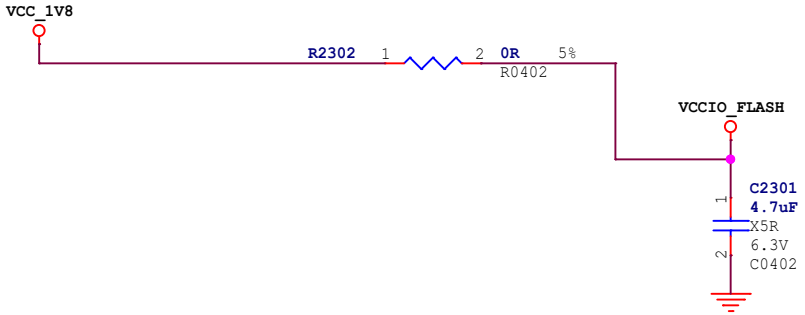
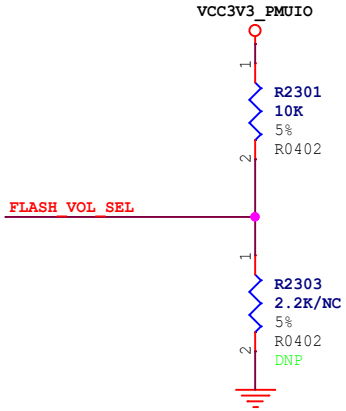
FLASH_VOL_SEL

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

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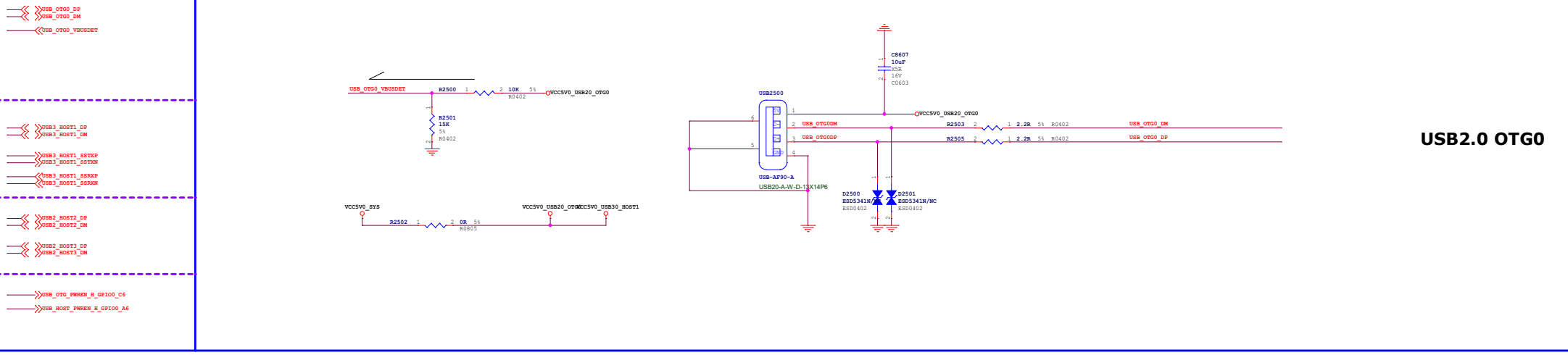
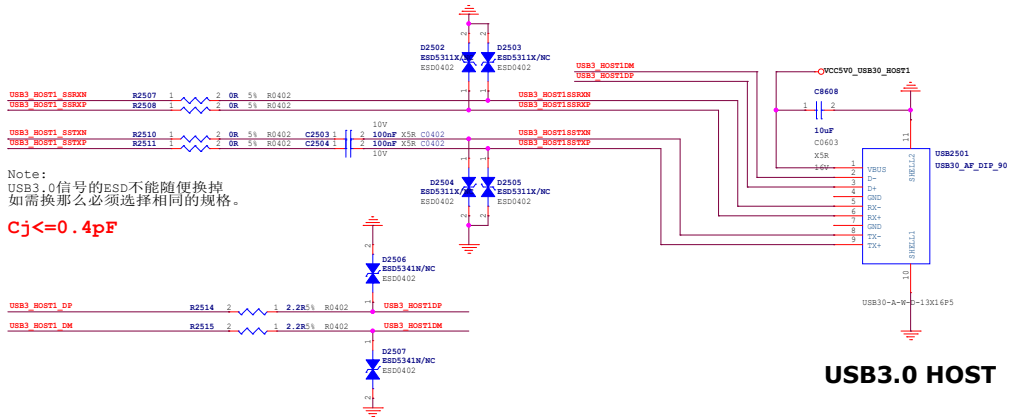
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	23.Power_Flash Power Manage				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 35

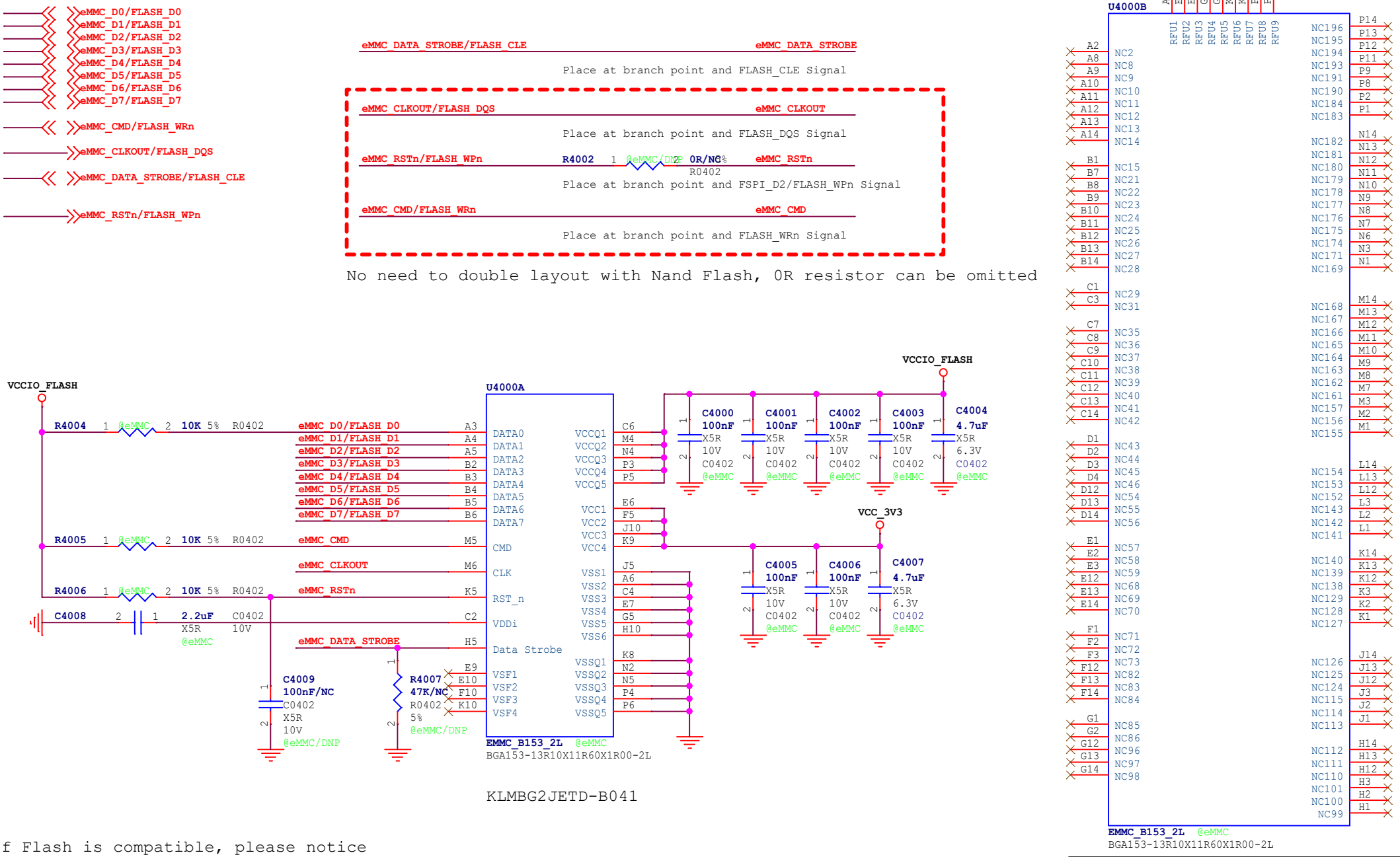


USB2.0 OTG0



USB3.0 HOST

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3566_BOX_Demo1_DDR4P408DD4
File:	25.USB2/USB3 Port
Date:	Wednesday, March 24, 2021
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	21 of 35



If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

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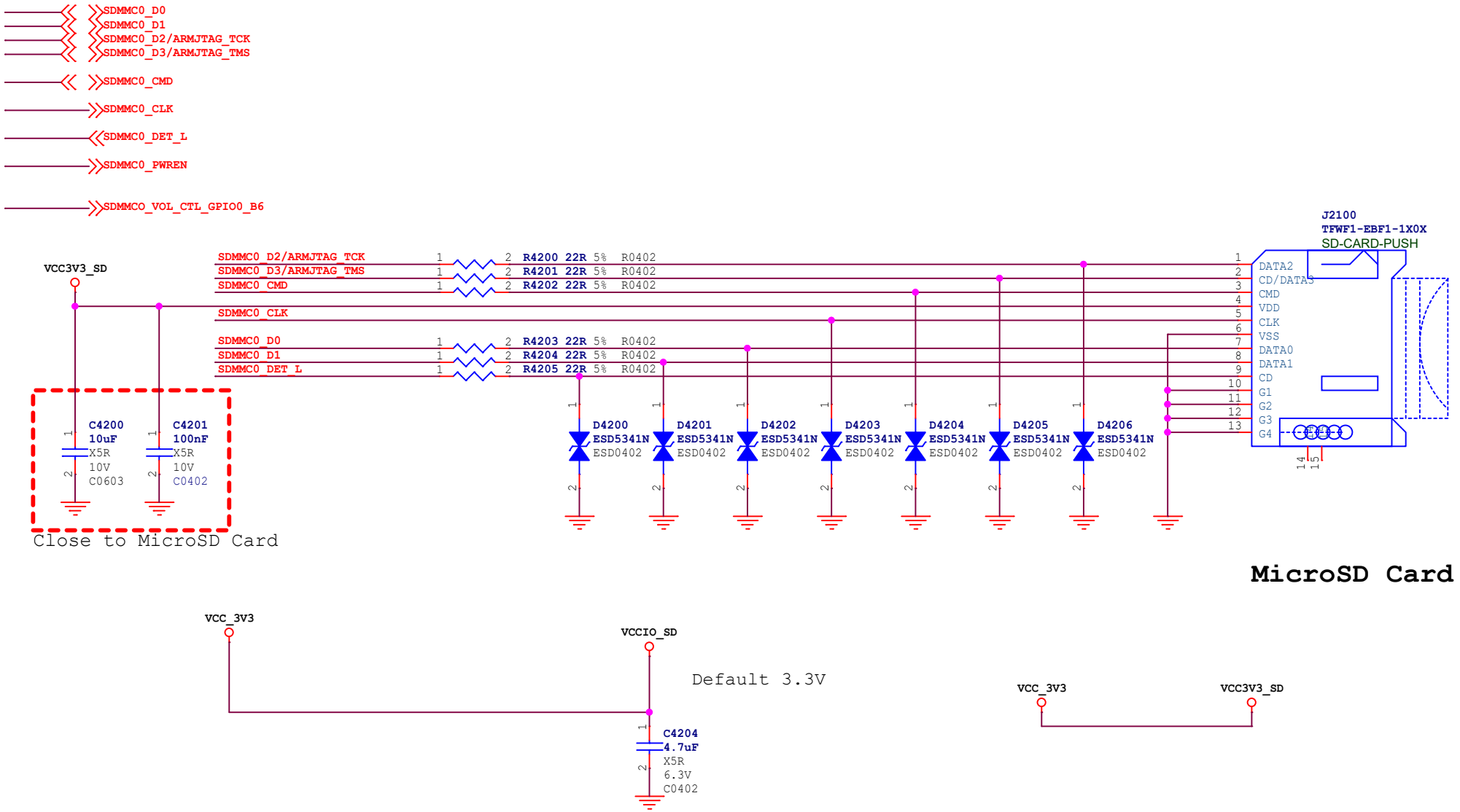
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	40.Flash-eMMC Flash				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	23 of 35



SDIO2.0 H; 3.26V
SDIO3.0 L; 1.8V
Default HIGH

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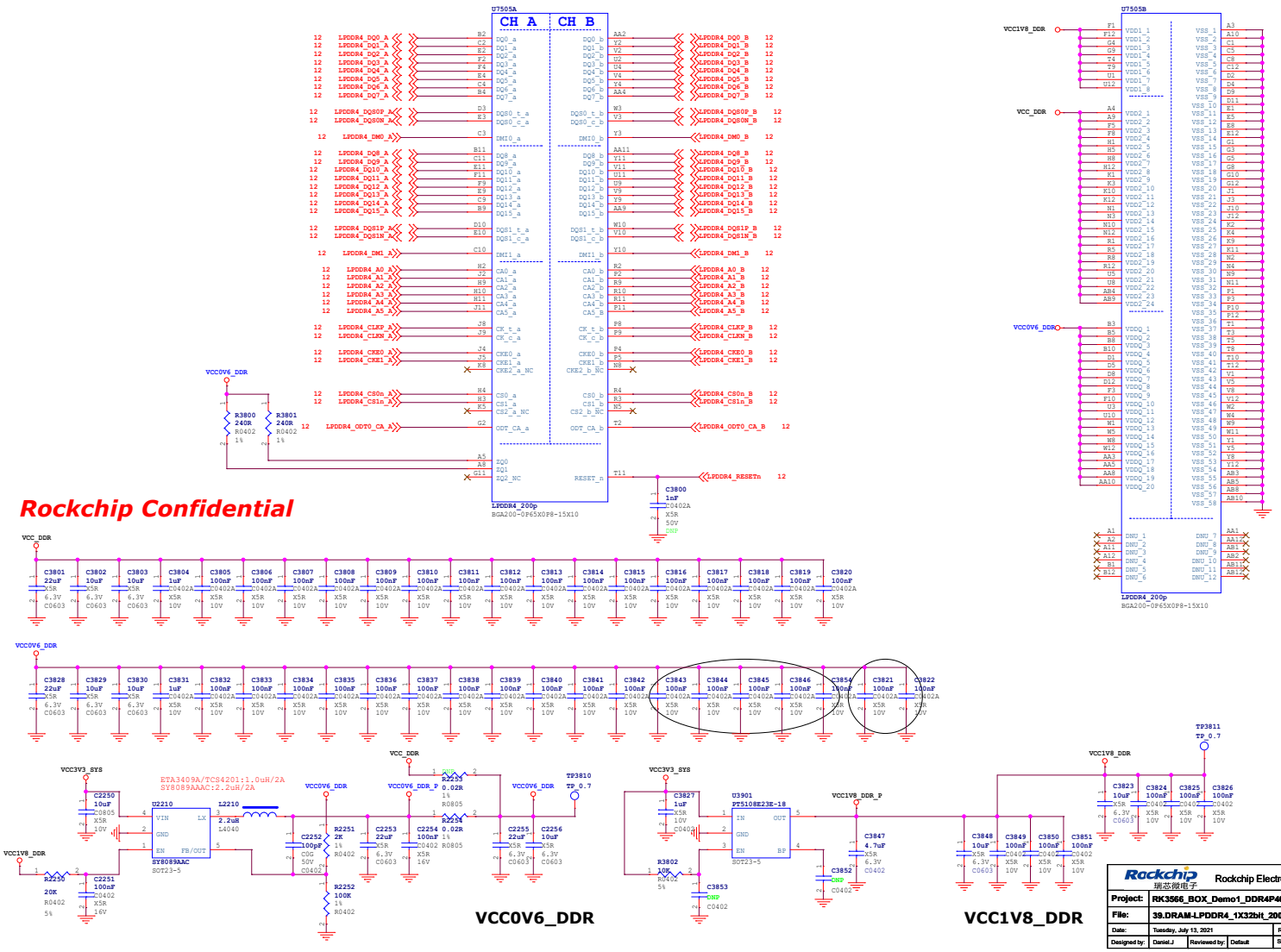
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	42.Flash-MicroSD Card				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	25 of 35



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VCC0V6_DDR

VCC1V8_DDR

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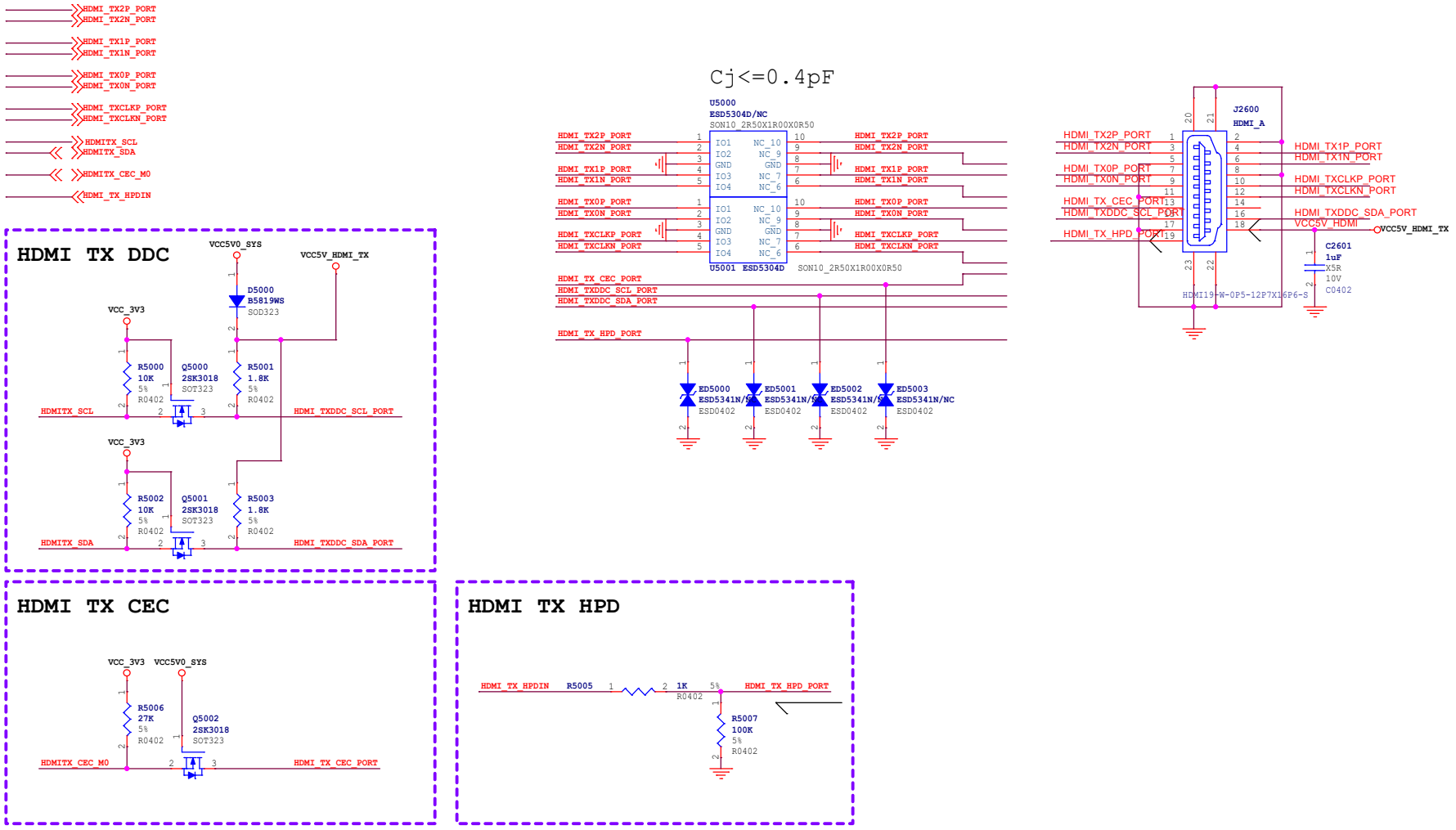
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	39.DRAM-LPDDR4_1X32bit_200P				
Date:	Tuesday, July 13, 2021			Rev:	V1.0
Designed by:	Daniel.J	Reviewed by:	Default	Sheet:	26 of 48



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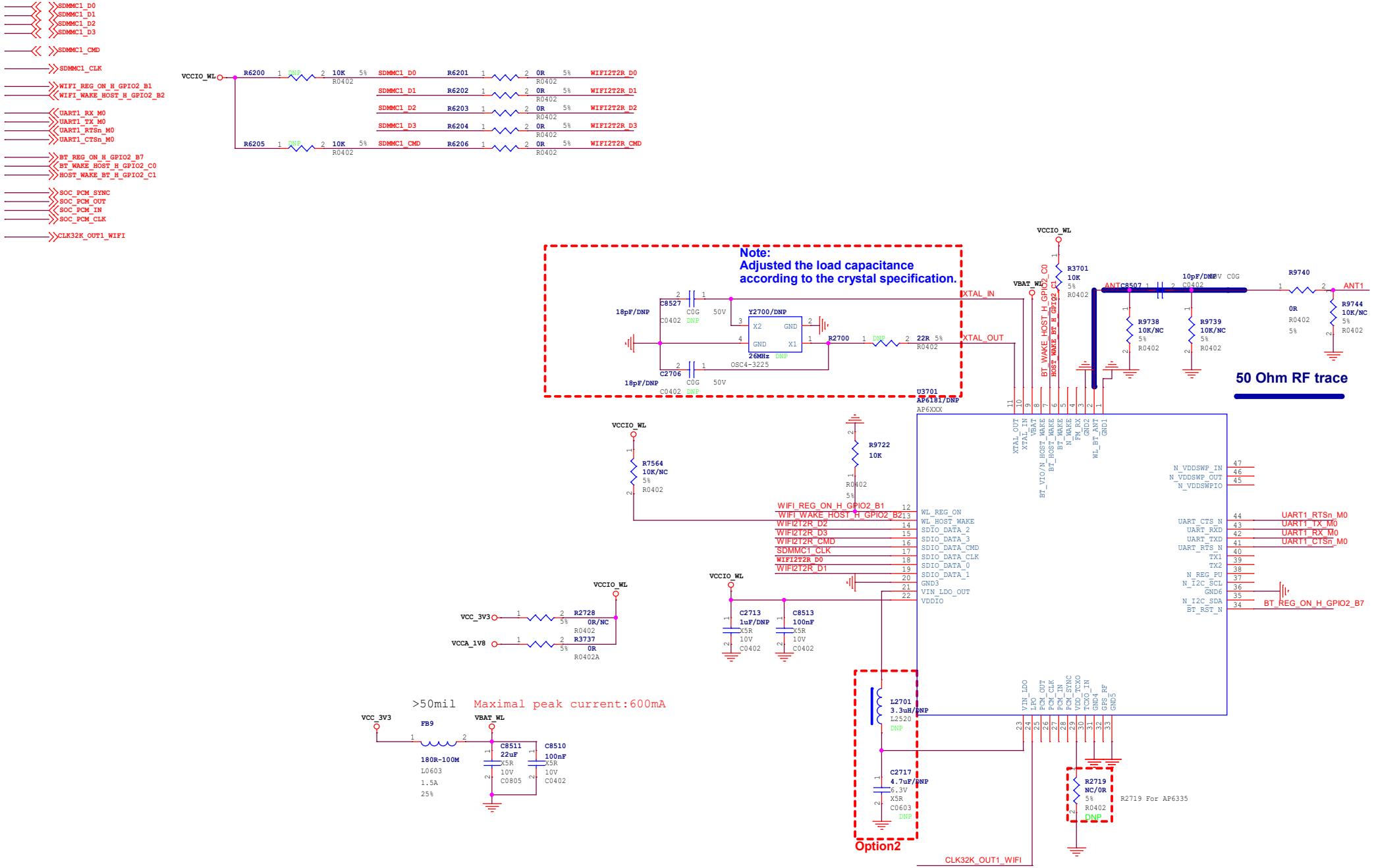
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	50.VO-HDMI2.0 TX				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	28 of 35



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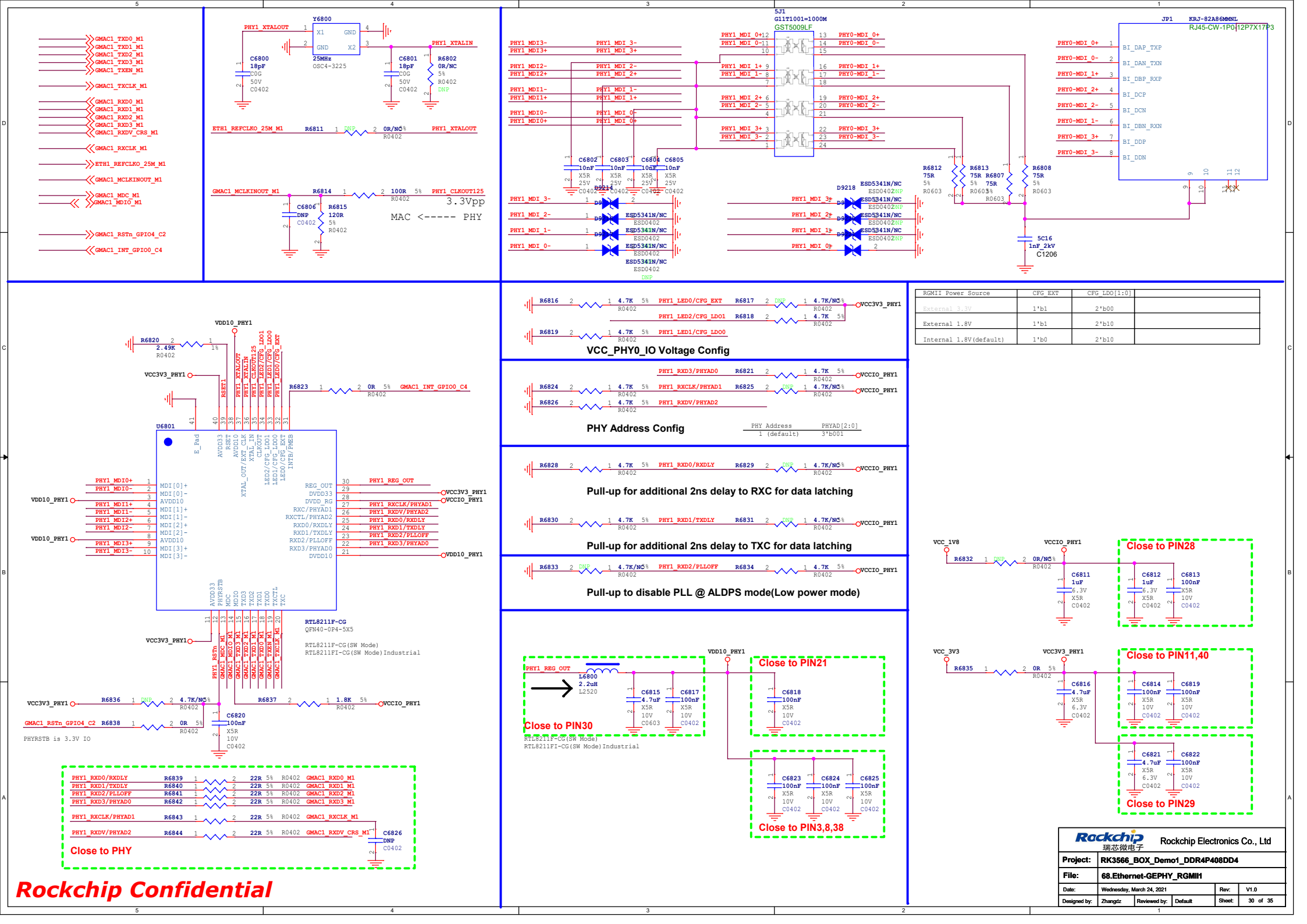
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	62.WIFI/BT-SDIO1_2T2R + UART				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	29 of 35


GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO4_C2
GMAC1_INT_GPIO0_C4
Y6800
PHY1_XTALOUT
PHY1_XTALIN
25MHz
OSC4-3225
C6800 18pF C0G 50V C0402
C6801 18pF C0G 50V C0402
R6802 0R/NC 5% R0402 DNP
ETH1_REFCLKO_25M_M1 R6811 DNP 0R/NC% R0402 PHY1_XTALOUT
GMAC1_MCLKINOUT_M1 R6814 100R 5% R0402 PHY1_CLKOUT125
3.3Vpp
MAC <----- PHY
C6806 DNP C0402
R6815 120R 5% R0402
5J1
G11T1001=1000M
GST5009LF
PHY1_MDI3- PHY1_MDI3+
PHY1_MDI2- PHY1_MDI2+
PHY1_MDI1- PHY1_MDI1+
PHY1_MDI0- PHY1_MDI0+
PHY0-MDI_0+ PHY0-MDI_0-
PHY0-MDI_1+ PHY0-MDI_1-
PHY0-MDI_2+ PHY0-MDI_2-
PHY0-MDI_3+ PHY0-MDI_3-
C6802 C6803 C6804 C6805 10nF X5R 25V C0402
D9214 D9215 D9216 D9217 ESD5341N/NC ESD0402
D9218 ESD5341N/NC ESD0402 DNP
R6812 75R 5% R0603
R6813 75R R6807 75R 5% R0603
R6808 75R 5% R0603
5C16 1nF_2kV C1206
JP1 KRJ-82A86MNL RJ45-CW-1P0-12P7X17P3
BI_DAP_TXP
BI_DAN_TXN
BI_DBP_RXP
BI_DCP
BI_DCN
BI_DBN_RXN
BI_DDP
BI_DDN
VDD10_PHY1
VCC3V3_PHY1
R6820 2.49K 1% R0402
R6823 0R 5% R0402 GMAC1_INT_GPIO0_C4
U6801
E_Pad
RSET1
PHY1_XTALOUT
PHY1_XTALIN
PHY1_CLKOUT125
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
PHY1_LED0/CFG_EXT
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY1_REG_OUT
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
PHY1_RSTn GMAC1_MDC_M1 GMAC1_MDIO_M1 GMAC1_TXD3_M1 GMAC1_TXD2_M1 GMAC1_TXD1_M1 GMAC1_TXD0_M1 GMAC1_TXEN_M1 GMAC1_TXCLK_M1
RTL8211F-CG
QFN40-0P4-5X5
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
R6836 DNP 4.7K/NC% R0402
R6837 1.8K 5% R0402
GMAC1_RSTn_GPIO4_C2 R6838 0R 5% R0402
PHYRSTB is 3.3V IO
C6820 100nF X5R 10V C0402
PHY1_RXD0/RXDLY R6839 22R 5% R0402 GMAC1_RXD0_M1
PHY1_RXD1/TXDLY R6840 22R 5% R0402 GMAC1_RXD1_M1
PHY1_RXD2/PLLOFF R6841 22R 5% R0402 GMAC1_RXD2_M1
PHY1_RXD3/PHYAD0 R6842 22R 5% R0402 GMAC1_RXD3_M1
PHY1_RXCLK/PHYAD1 R6843 22R 5% R0402 GMAC1_RXCLK_M1
PHY1_RXDV/PHYAD2 R6844 22R 5% R0402 GMAC1_RXDV_CRS_M1
C6826 DNP C0402
Close to PHY
R6816 4.7K 5% R0402 PHY1_LED0/CFG_EXT
R6817 DNP 4.7K/NC% R0402 VCC3V3_PHY1
PHY1_LED2/CFG_LDO1 R6818 4.7K 5% R0402
R6819 4.7K 5% R0402 PHY1_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config
R6821 4.7K 5% R0402 VCCIO_PHY1
R6824 4.7K 5% R0402 PHY1_RXD3/PHYAD0
R6825 DNP 4.7K/NC% R0402 VCCIO_PHY1
R6826 4.7K 5% R0402 PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
PHY Address Config
PHY Address 1 (default) PHYAD[2:0] 3'b001
R6828 4.7K 5% R0402 PHY1_RXD0/RXDLY
R6829 DNP 4.7K/NC% R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to RXC for data latching
R6830 4.7K 5% R0402 PHY1_RXD1/TXDLY
R6831 DNP 4.7K/NC% R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to TXC for data latching
R6833 DNP 4.7K/NC% R0402 PHY1_RXD2/PLLOFF
R6834 4.7K 5% R0402 VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
PHY1_REG_OUT
L6800 2.2uH L2520
C6815 4.7uF X5R 10V C0603
C6817 100nF X5R 10V C0402
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C6818 100nF X5R 10V C0402
Close to PIN21
C6823 100nF X5R 10V C0402
C6824 100nF X5R 10V C0402
C6825 100nF X5R 10V C0402
Close to PIN3,8,38
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V(default) | 1'b0 | 2'b10
VCC_1V8
R6832 DNP 0R/NC% R0402
C6811 1uF 6.3V X5R C0402
C6812 1uF 6.3V X5R C0402
C6813 100nF X5R 10V C0402
Close to PIN28
VCC_3V3
R6835 0R 5% R0402
C6816 4.7uF X5R 6.3V C0402
C6814 100nF X5R 10V C0402
C6819 100nF X5R 10V C0402
Close to PIN11,40
C6821 4.7uF X5R 6.3V C0402
C6822 100nF X5R 10V C0402
Close to PIN29
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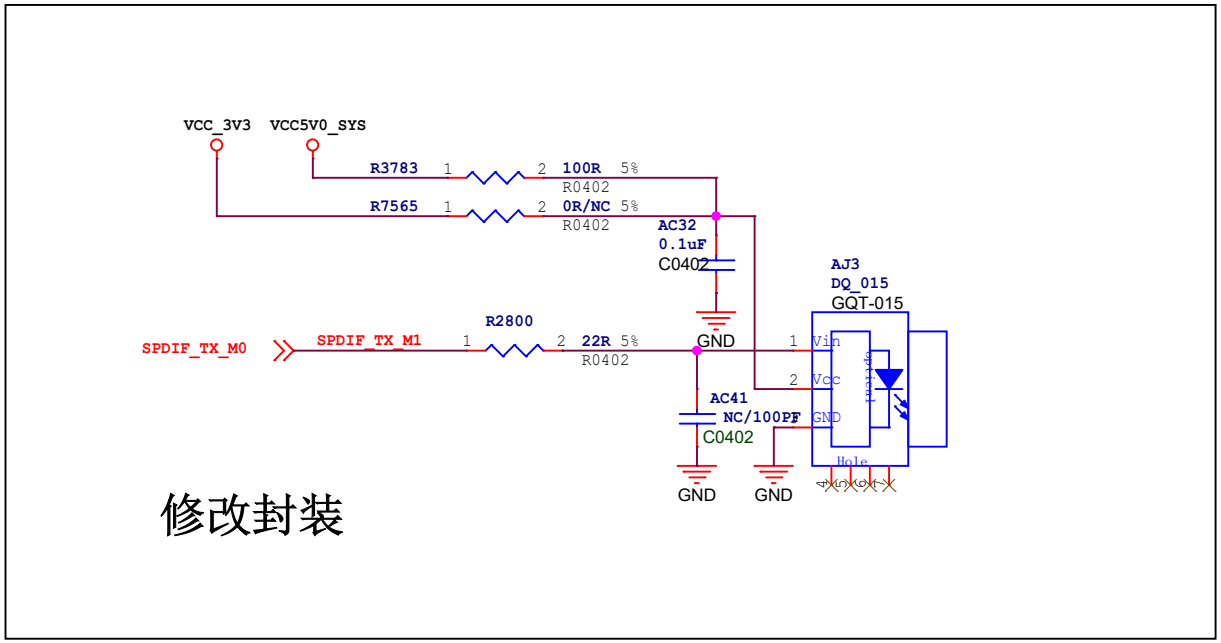
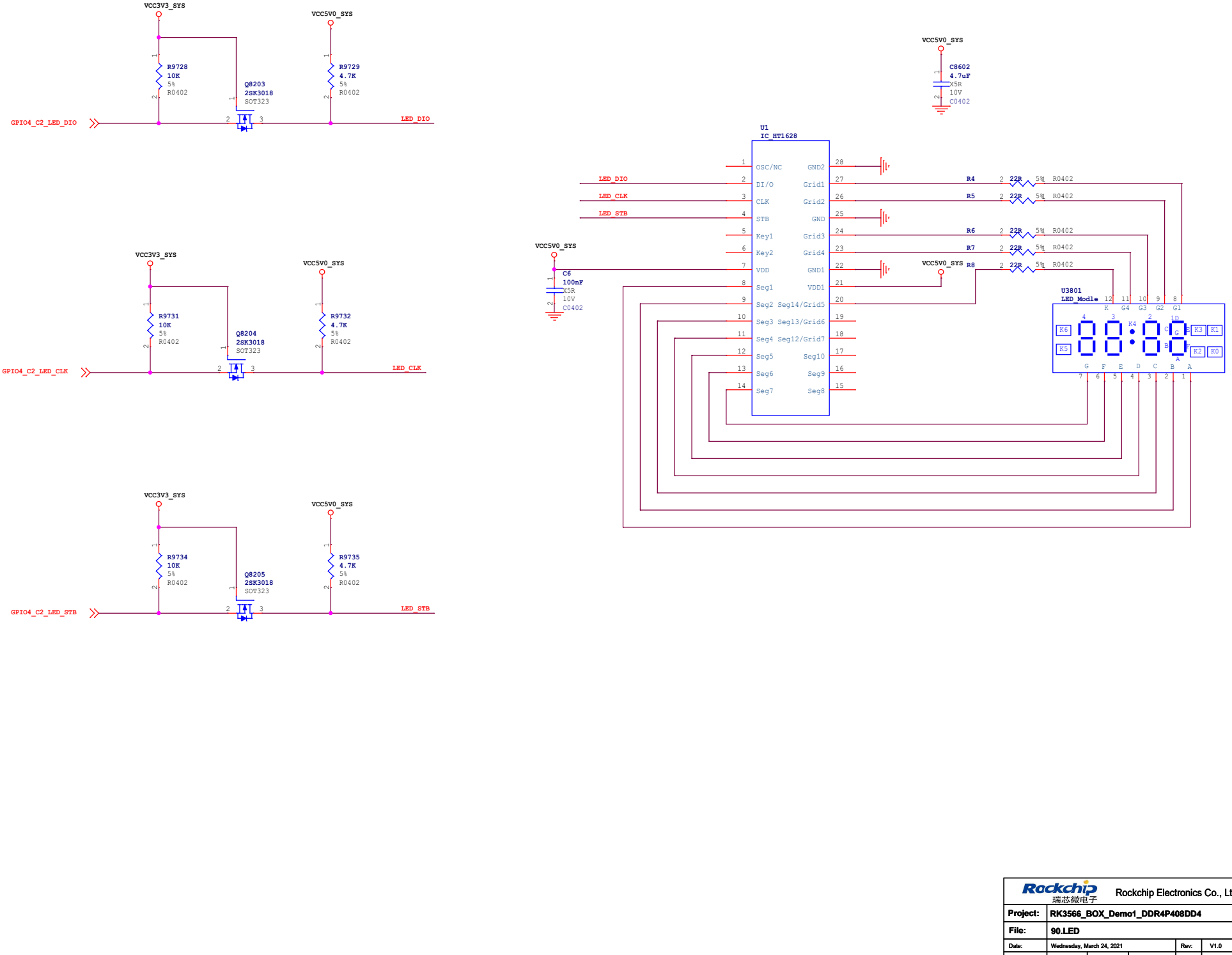
Rockchip Electronics Co., Ltd
Project: RK3566_BOX_Demo1_DDR4P408DD4
File: 68.Ethernet-GEPHY_RGMII
Date: Wednesday, March 24, 2021
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 30 of 35

SPDIF_TX_M0



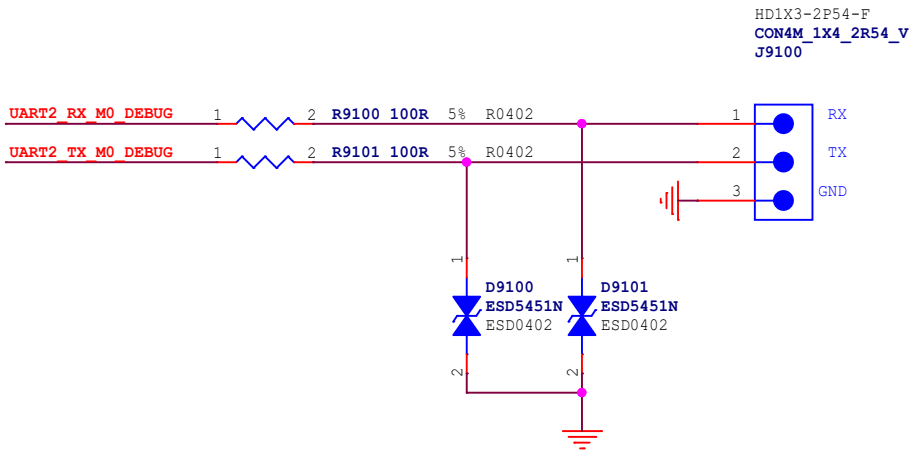
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	76.Audio-S/PDIF TX Port				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	31 of 35



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	90.LED				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	33 of 35

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	91.Debug UART				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	34 of 35

TOP Mark

BOTTOM Mark

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3566_BOX_Demo1_DDR4P408DD4				
File:	99.Mark/Hole/Heatsink				
Date:	Wednesday, March 24, 2021			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	35 of 35