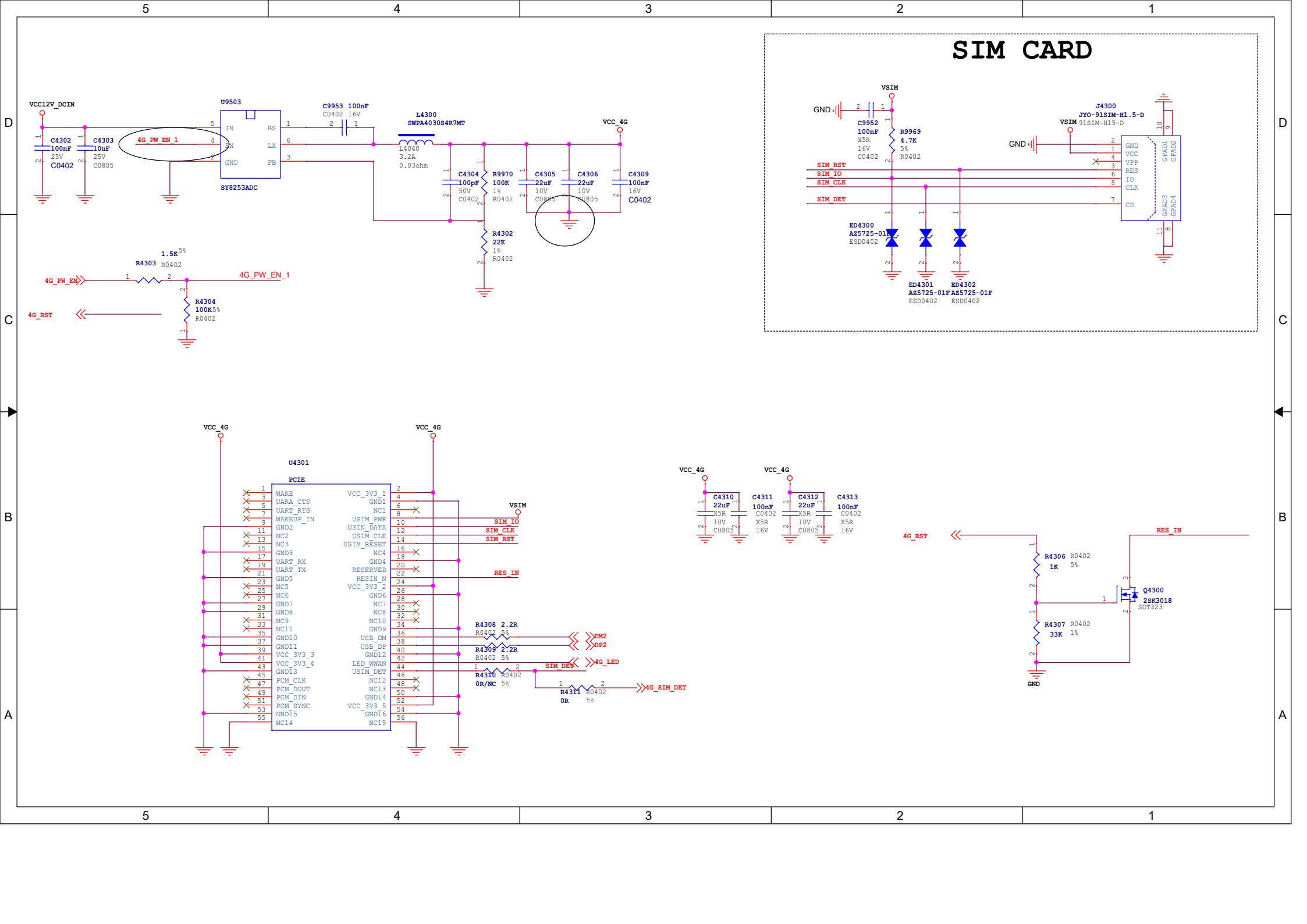

SIM CARD
VCC12V_DCIN
U9503
SY8253ADC
4G_PW_EN_1
L4300
SWPA4030S4R7MT
VCC_4G
4G_PW_EN
4G_RST
VSIM
GND
SIM_RST
SIM_IO
SIM_CLK
SIM_DET
J4300
JYO-91SIM-H1.5-D
U4301
PCIE
RES_IN
4G_LED
4G_SIM_DET
Q4300
2SK3018
SOT323

Schematics Only for RK3588 NVR

RK_NVR_DEMO1_RK3588_LP4XD200P232SD8_V21

Main Functions Introduction

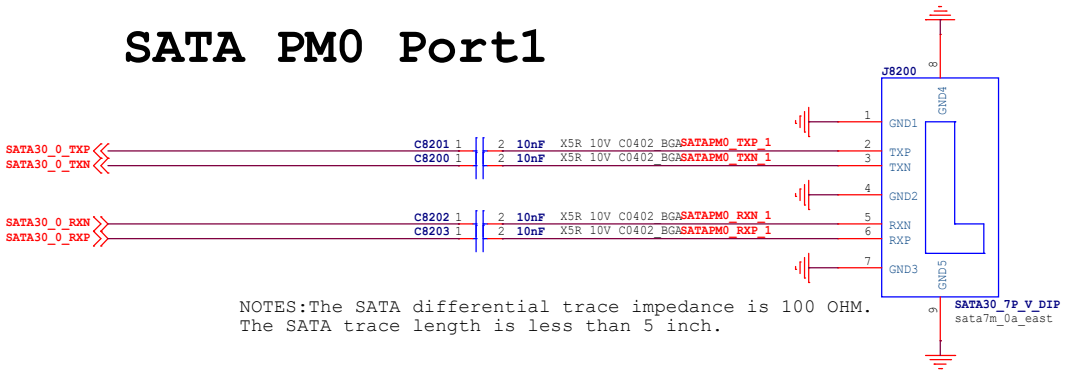
1) PMIC: RK806-1+DiscretePower
2) RAM: 2 x LPDDR4x 32bit(Option 2 x LPDDR4 32bit)
3) ROM: eMMC5.1(Option SPI Nand Falsh)
4) Support: 1 x TypeC(With DP TX)
5) Support: 1 x USB3.0 HOST + 2 x USB2.0 HOST
6) Support: 10 x SATA3.0 Connector (7pin)
7) Support: 1 x 4Lanes PCIe Connector
8) Support: 2 x HDMI2.1 TX + 1 x HDMI2.0 TX + 1 x HDMI1.4 TX
9) Support: 2 x 4Lanes MIPI CSI RX Camera Connector
10) Support: 2 x 10/100/1000 Ethernet(RGMII)
11) Support: 1 x Line Out, 1 x Line In
12) Support: 1 x Buzzer
13) Support: 1 x IR Receiver
14) Support: 1 x Power LED,1 x Ethernet LED,1 x HDD LED
15) Support: 1 x Recovery Key,1x Reset Key
16) Support: 1 x RS232
17) Support: 1 x RS485
18) Support: 1 x UART
19) Support: Debug UART(USB to UART),Debug JTAG (4Pin)

Note:

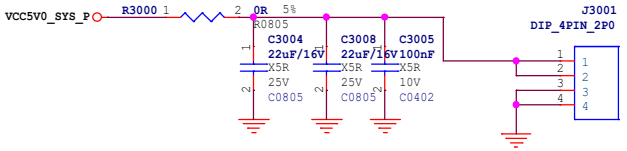
The RK806 LDO power distribution of the reference schematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	00.Cover Page				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	1 of 43

SATA PM0 Port1



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.



ShenZhen HugSun Technology Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	82. SATA3.0		
Date:	Thursday, September 15, 2022	Rev:	V1.0
Designed by:	Wang	Sheet:	1 of 99

Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

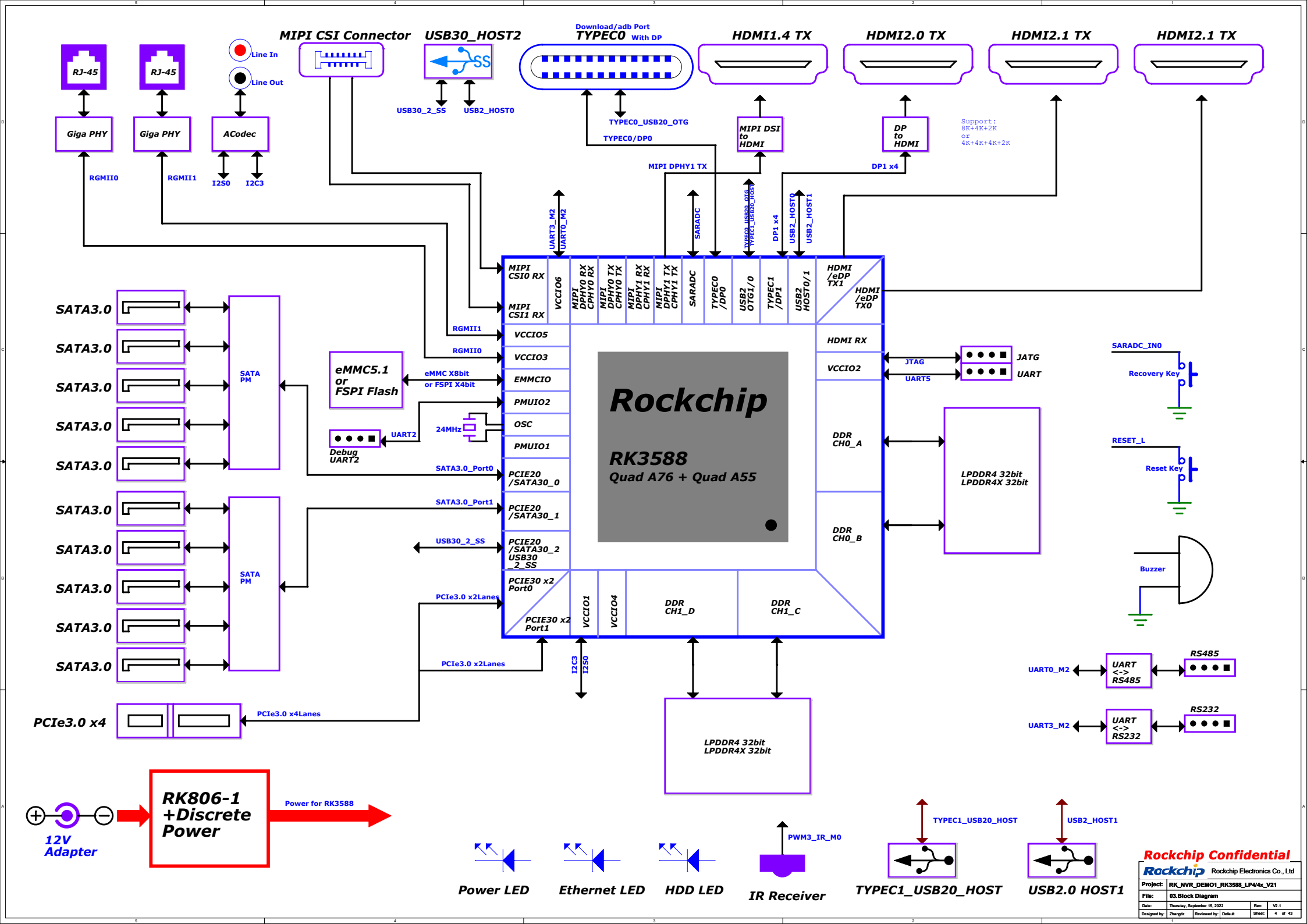
NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	01.Index and Notes				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	2 of 43

Revision History

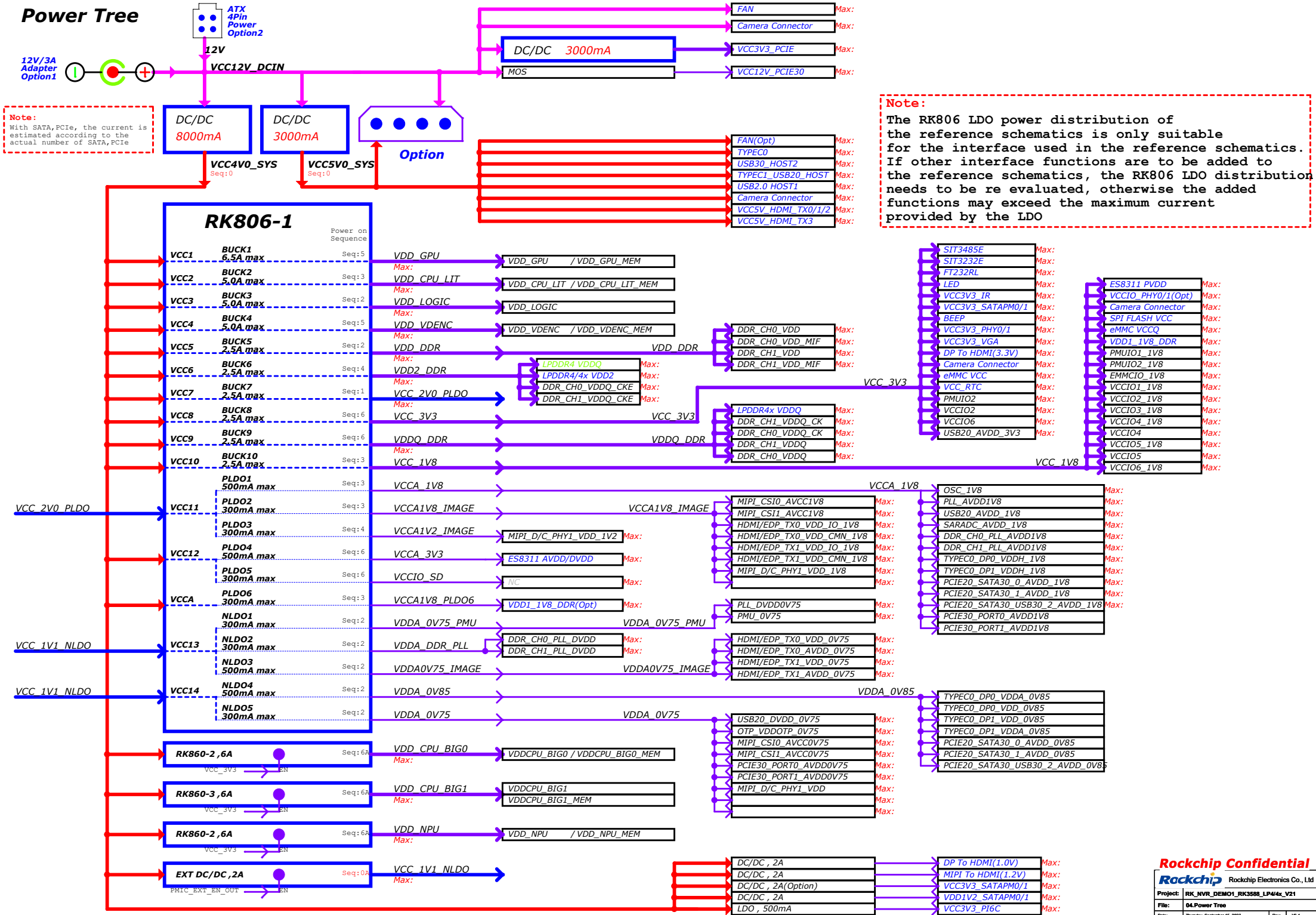
Version	Date	By	Change Dsecription	Approved
V1.0	2021-09-24	Zhangdz	1:Revision preliminary version	
V2.0	2021-12-08	Zhangdz	1:Invalid version	
V2.1	2021-12-28	Zhangdz	1:Change content Please Refer to: RK_NVR_DEMO1_RK3588_LP4XD200P232SD8_V21_20211228_Modify_Notes_CN	



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	03.Block Diagram
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	4 of 43

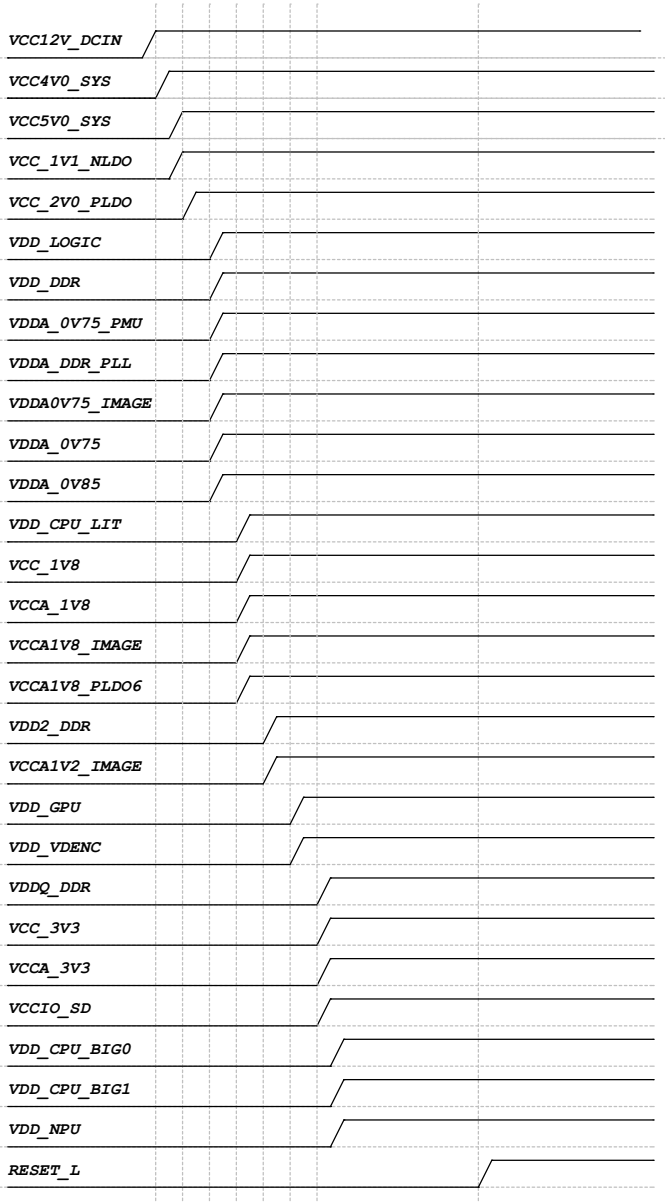
Power Tree



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	04.Power Tree
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	5 of 43

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC4V0_SYS	RK806_BUCK1	6.5A	VDD_GPU	Slot:5	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK2	5A	VDD_CPU_LIT	Slot:3	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK3	5A	VDD_LOGIC	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC4V0_SYS	RK806_BUCK4	5A	VDD_VDENC	Slot:5	0.75V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK5	2.5A	VDD_DDR	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC4V0_SYS	RK806_BUCK6	2.5A	VDD2_DDR	Slot:4	ADJ FB=0.5V	ON	1.1V LPDDR4/4x	TBD	TBD
VCC4V0_SYS	RK806_BUCK7	2.5A	VCC_2V0_PLDO	Slot:1	2.0V	ON	2.0V	TBD	TBD
VCC4V0_SYS	RK806_BUCK8	2.5A	VCC_3V3	Slot:6	3.3V	ON	3.3V	TBD	TBD
VCC4V0_SYS	RK806_BUCK9	2.5A	VDDQ_DDR	Slot:6	ADJ FB=0.5V	ON	0.6V LPDDR4/4x	TBD	TBD
VCC4V0_SYS	RK806_BUCK10	2.5A	VCC_1V8	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_IMAGE	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VCCA1V2_IMAGE	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC4V0_SYS	RK806_PLDO4	0.5A	VCCA_3V3	Slot:6	3.3V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD	Slot:6	3.3V	ON	3.3V	TBD	TBD
VCC4V0_SYS	RK806_PLDO6	0.3A	VCCA1V8_PLDO6	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDDA_0V75_PMU	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_IMAGE	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC12V_DCIN	EXT BUCK	8A	VCC4V0_SYS	Slot:0	4.0V	ON	4.0V	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO	Slot:0A	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_SYS	Slot:0A	5.2V	ON	5.2V	TBD	TBD
VCC4V0_SYS	RK860-2	6A	VDD_CPU_BIG0	Slot:6A	0.8V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK860-3	6A	VDD_CPU_BIG1	Slot:6A	0.8V	ON	DVFS	TBD	TBD
VCC4V0_SYS	RK860-2	6A	VDD_NPU	Slot:6A	0.8V	ON	DVFS	TBD	TBD

IO Power Domain Map

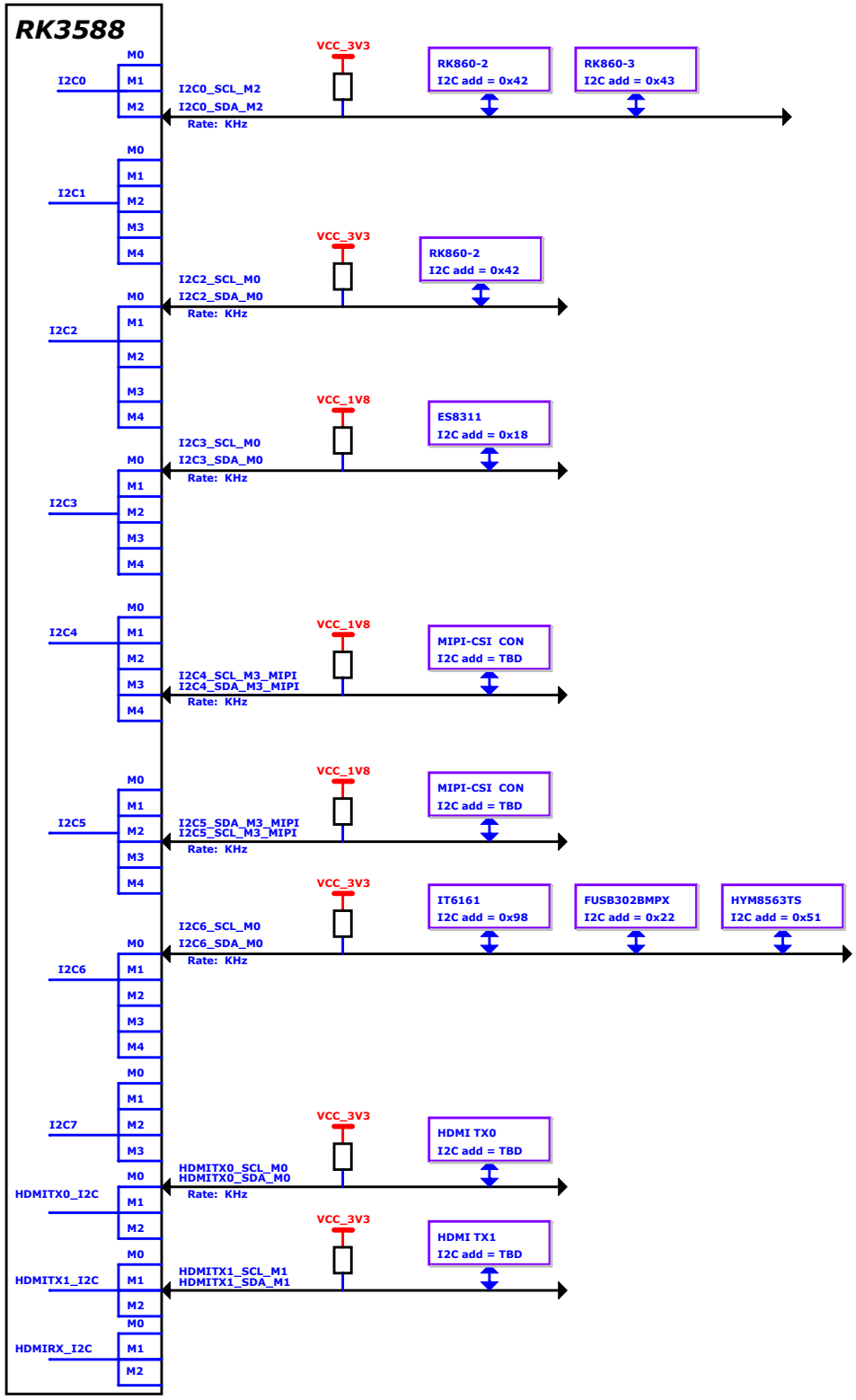
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8 VCC_3V3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8	1.8V
VCCIO1	Pin G20	1.8V Only	VDDIO1_1V8	VCC_1V8	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VDDIO2_1V8 VCCIO2	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin Y26	1.8V Only	VDDIO3_1V8	VCC_1V8	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VDDIO4_1V8 VCCIO4	VCC_1V8 VCC_1V8	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VDDIO5_1V8 VCCIO5	VCC_1V8 VCC_3V3	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VDDIO6_1V8 VCCIO6	VCC_1V8 VCC_3V3	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

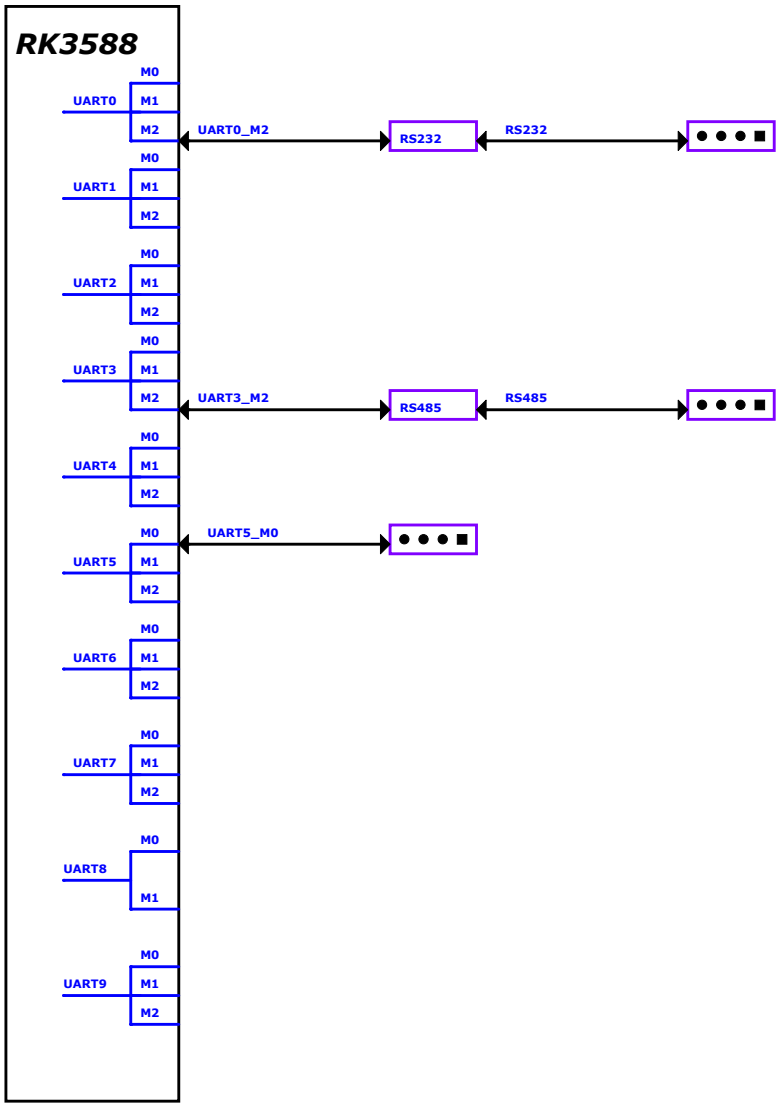
Rockchip Electronics Co., Ltd

Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	05.Power Sequence/IO Domain Map				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	6 of 43

I2C MAP



UART MAP



Rockchip Confidential

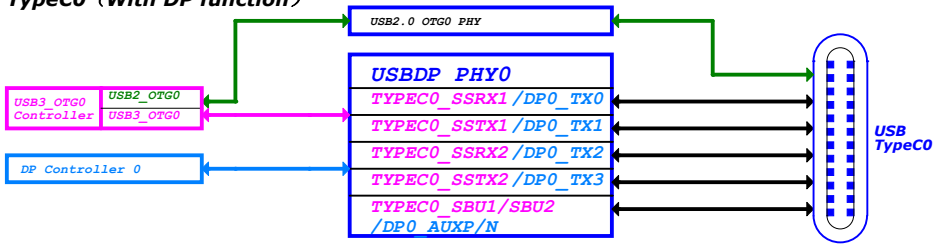
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	06.Lower-Speed Bus Map
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangdz
Reviewed by:	
Sheet:	7 of 43

USB Controller Configure Table

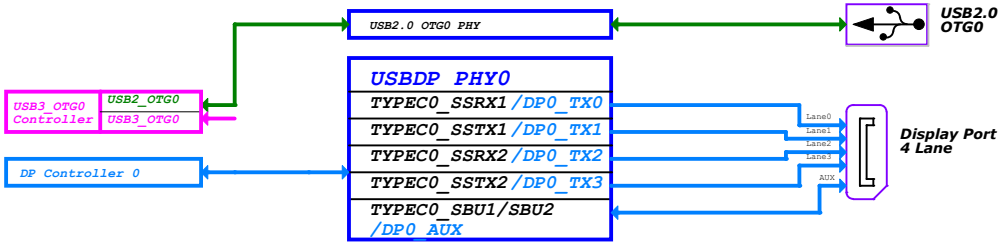
Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST	OPTION3 USB30 HOST				
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN				
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN				
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					
						TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM				

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

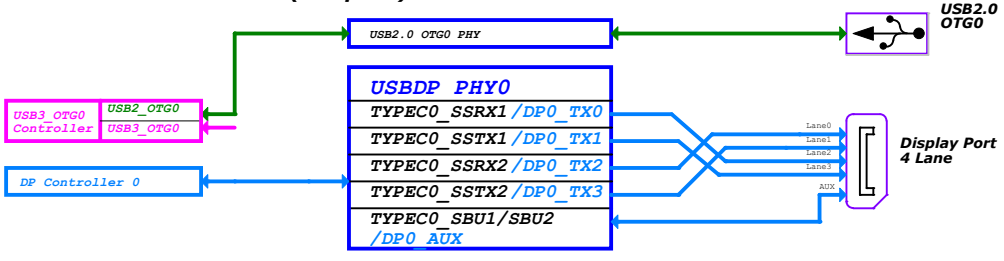
Config0:
TypeC0（With DP function）



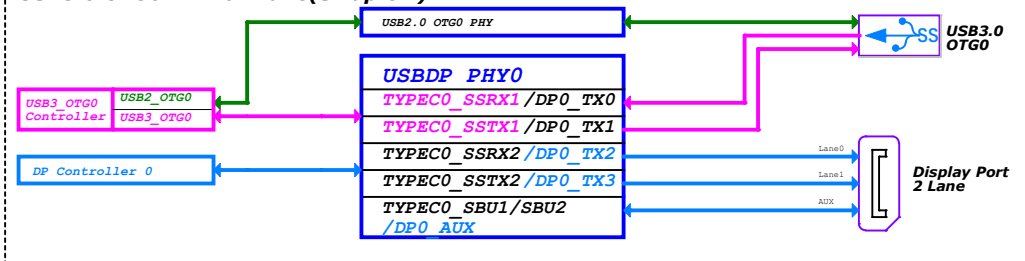
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



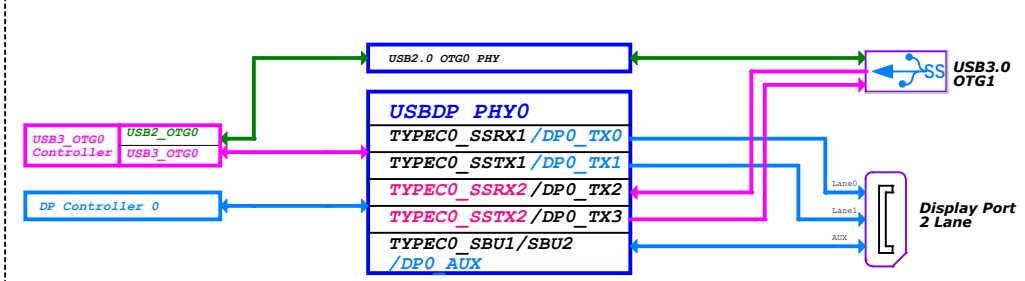
Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Config3:
USB3.0 OTG0 + DP0 2Lane(Swap ON)

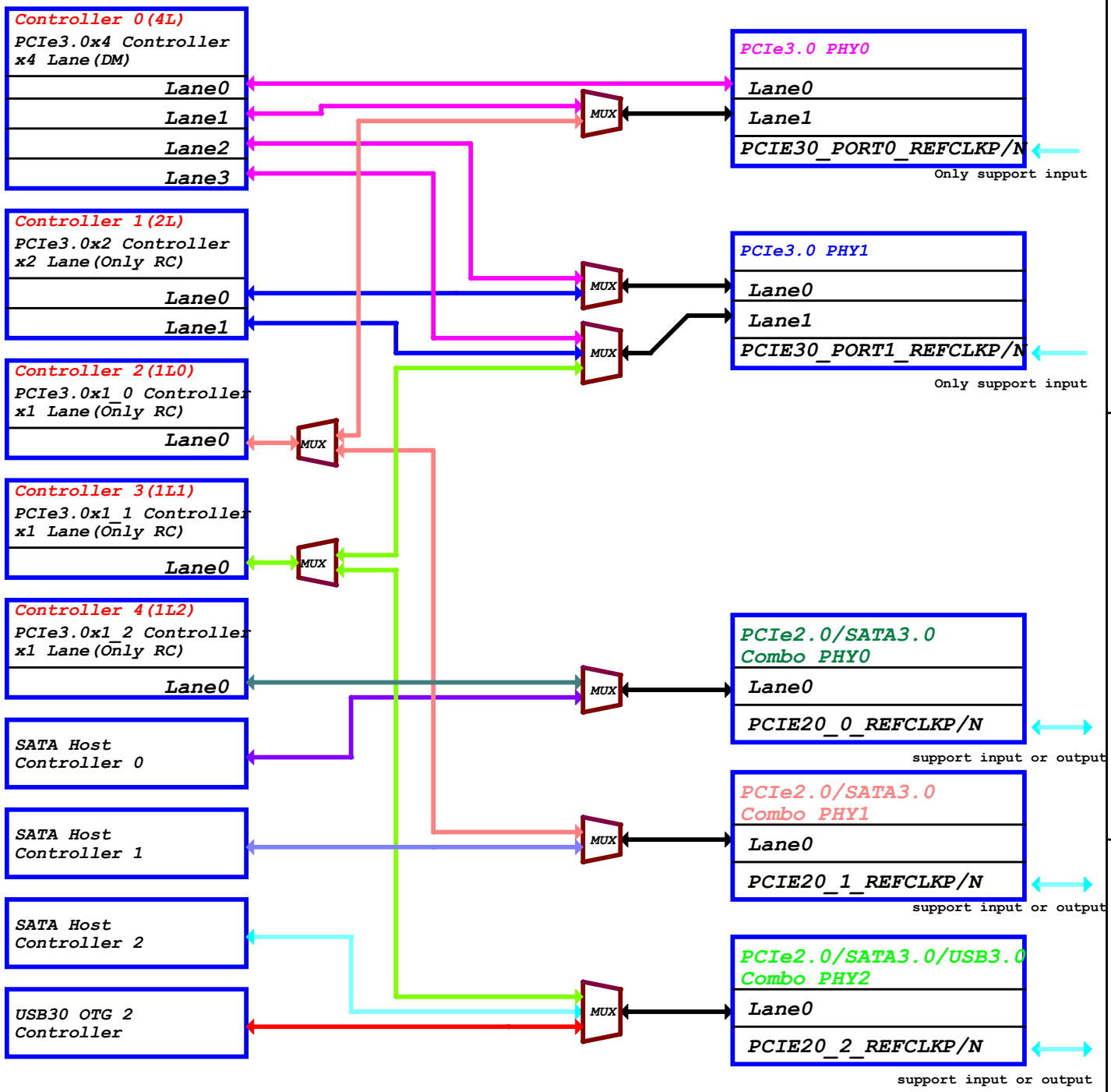


Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Rockchip Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21
File: 07.USB/DP Configure Map
Date: Thursday, September 10, 2020 Rev: V2.1
Designed by: Reviewed by: Sheet: 8 of 43

PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO & Power Pin
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

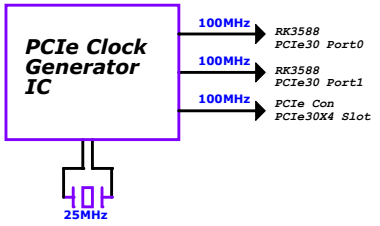
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

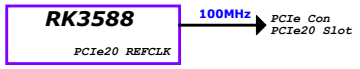
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK

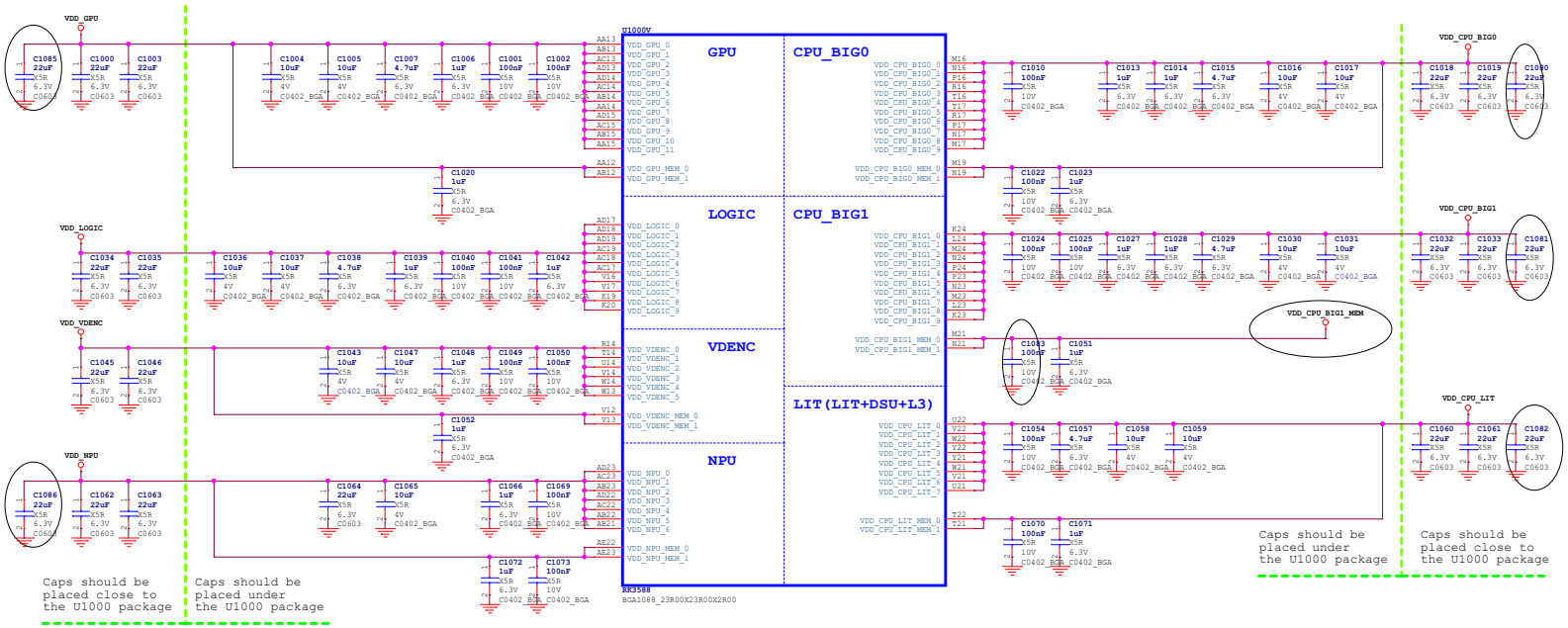


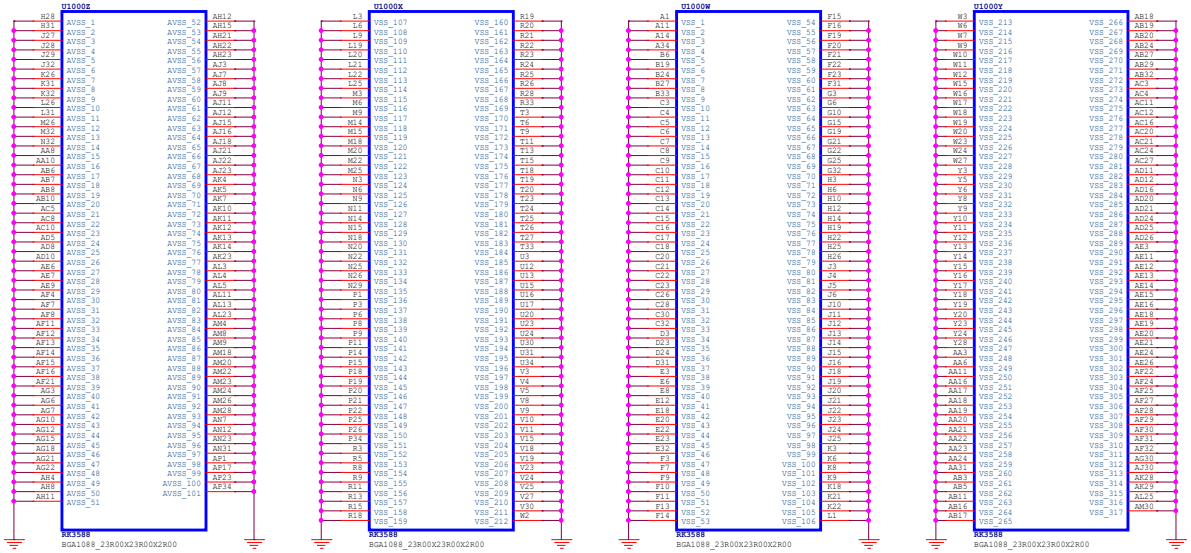
PCIe2.0 REFCLK



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	08.PCIE Fun Map		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by:	Zhangdt	Reviewed by:	Sheet: 9 of 43





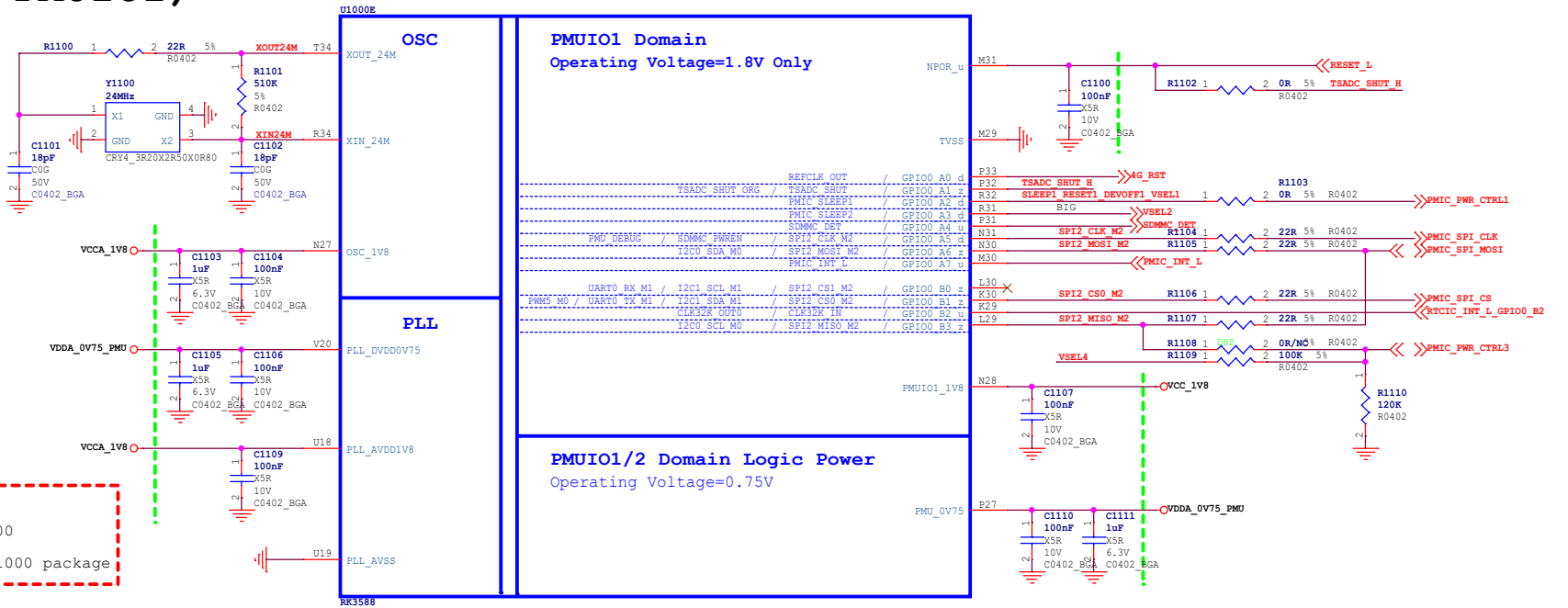
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	10.RK3588_Power/GND		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by:	Zhangdt	Reviewed by:	Sheet: 10 of 43

RK3588_E(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

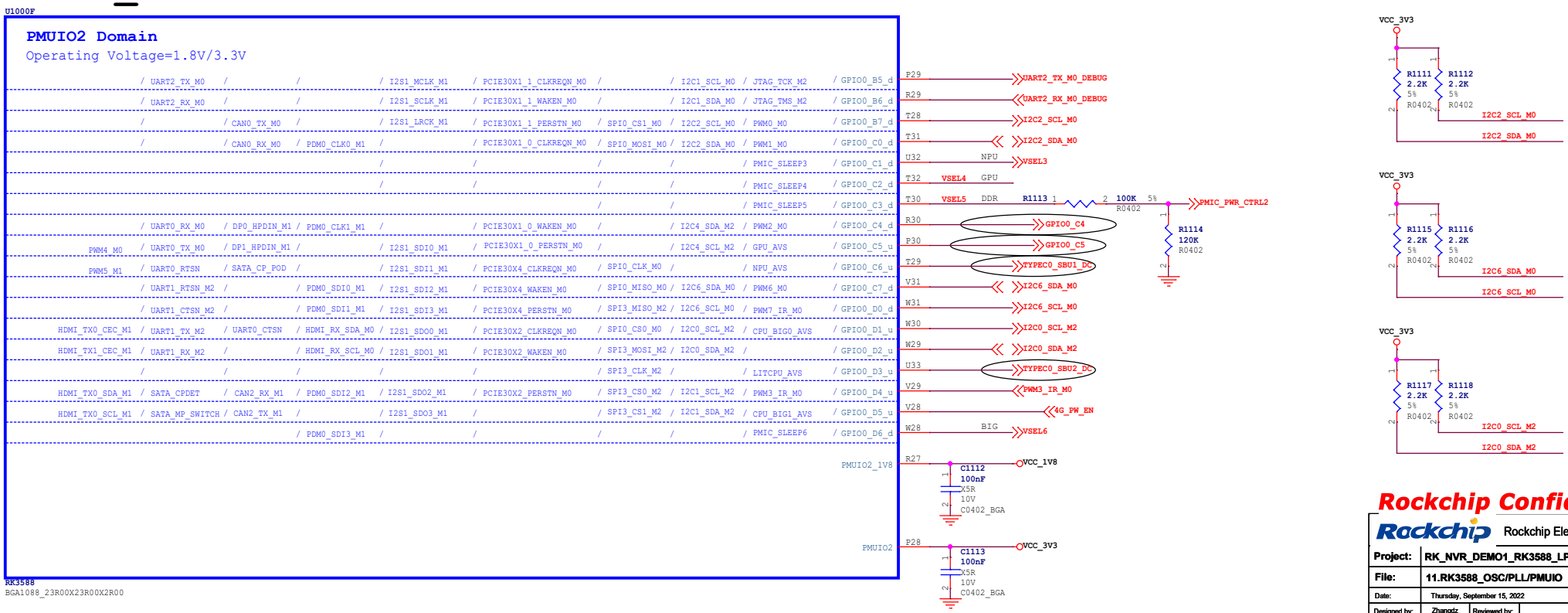
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<12pF



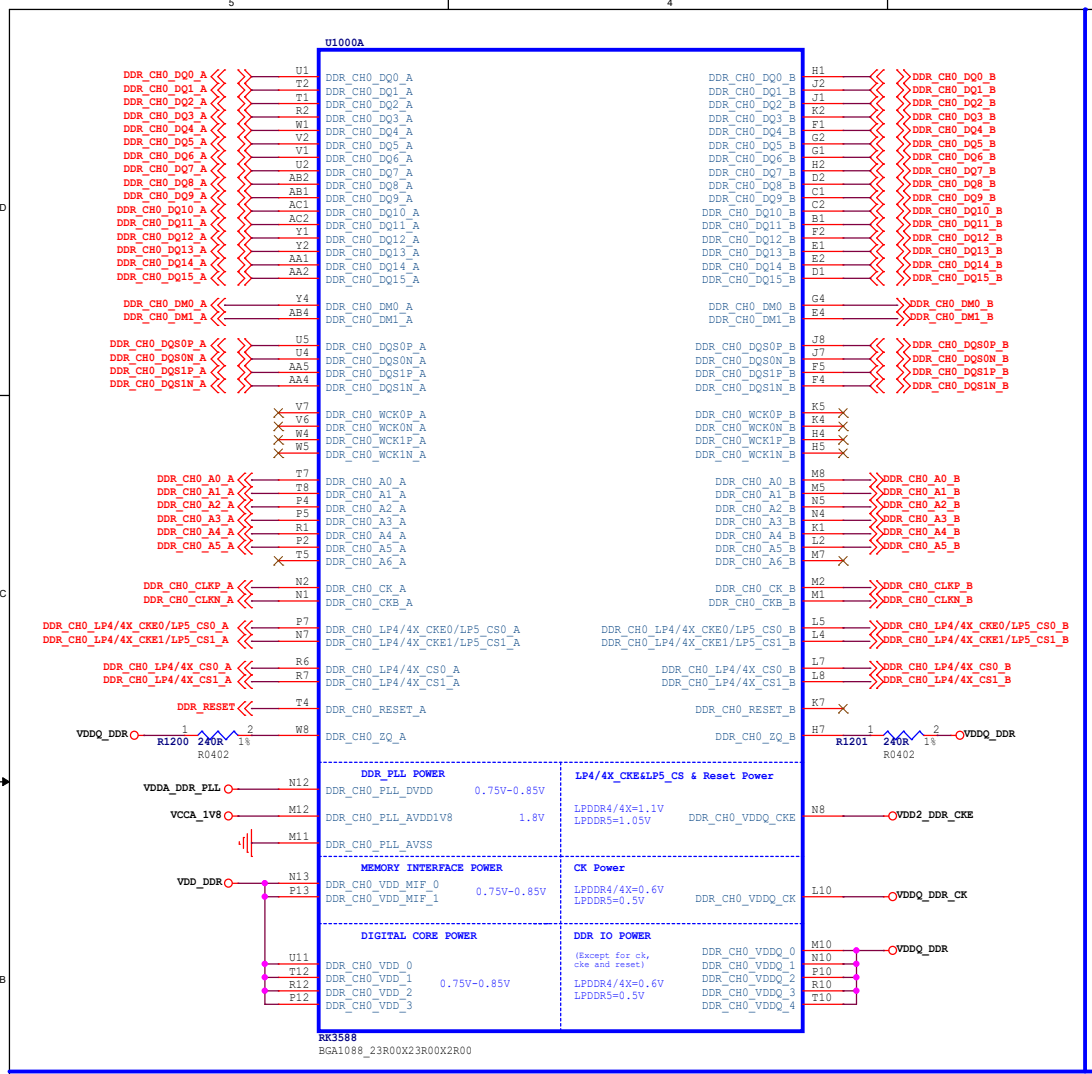
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

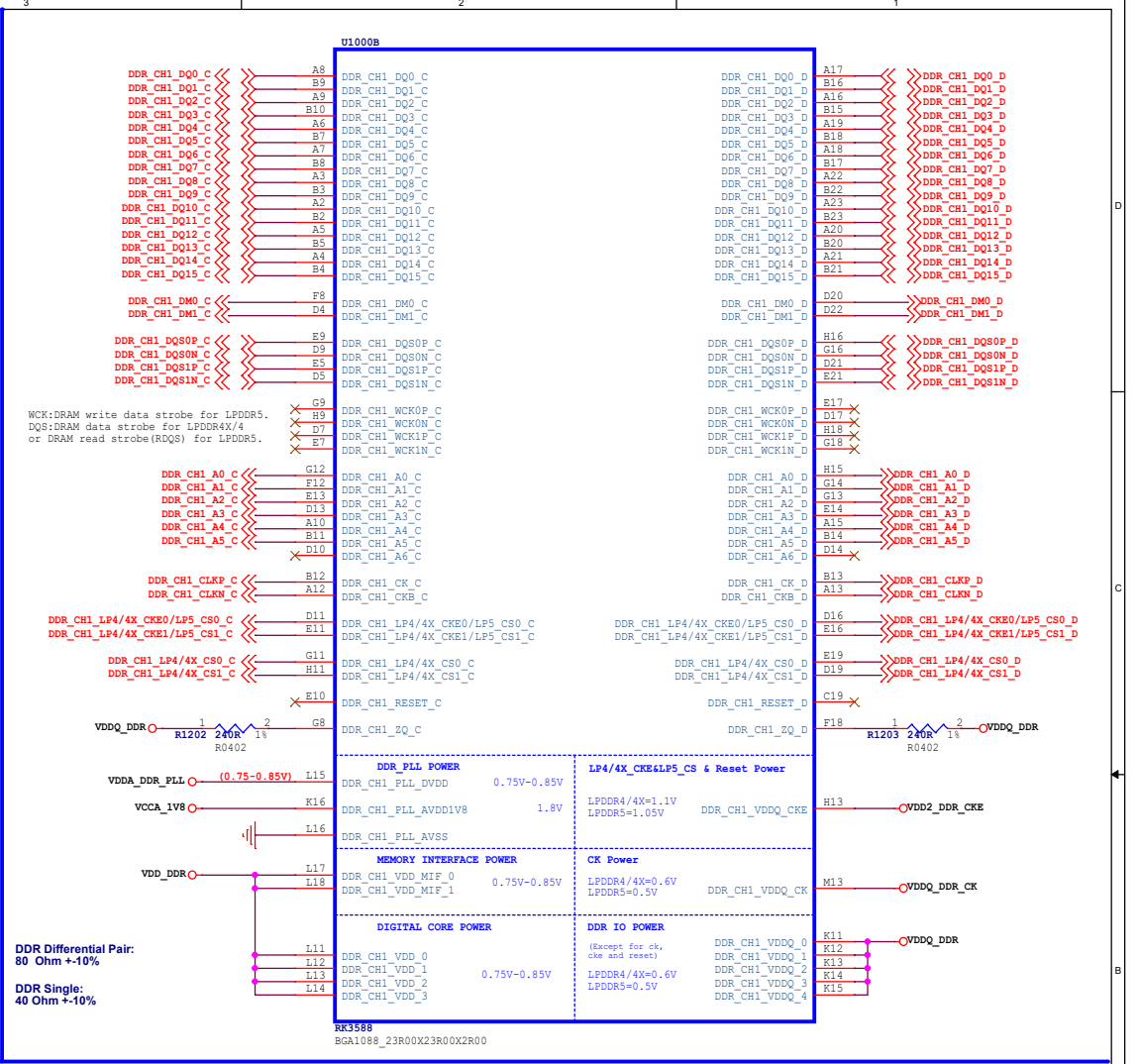
RK3588_F(PMUIO2)



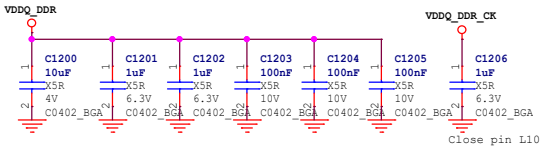
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	11.RK3588_OSC/PLL/PMUIO		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by: Zhangdz	Reviewed by:	Sheet:	11 of 43





DDR FILTER



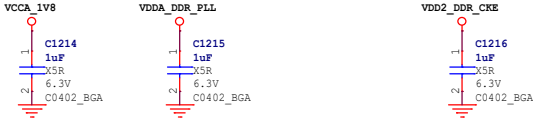
Hold power of CLK during retention times.

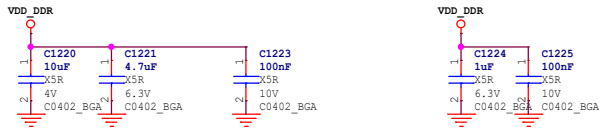
Sequence:
VDD-VDDQ_CKE-VDDQ

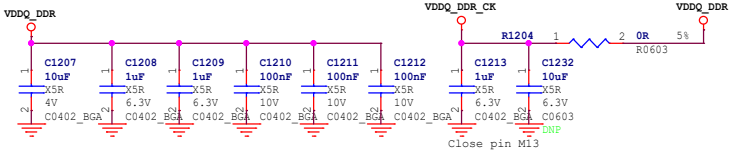
VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET,
lpddr4X=1.1V/lpddr5=1.05V

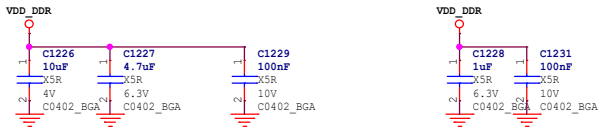
VDDQ_CK:power for CK,
LPDDR4/4X=0.6V/LPDDR5=0.5V

VDDQ:Power for DDR IO(except for ck, cke and reset);
LPDDR4/4X=0.6V/LPDDR5=0.5V



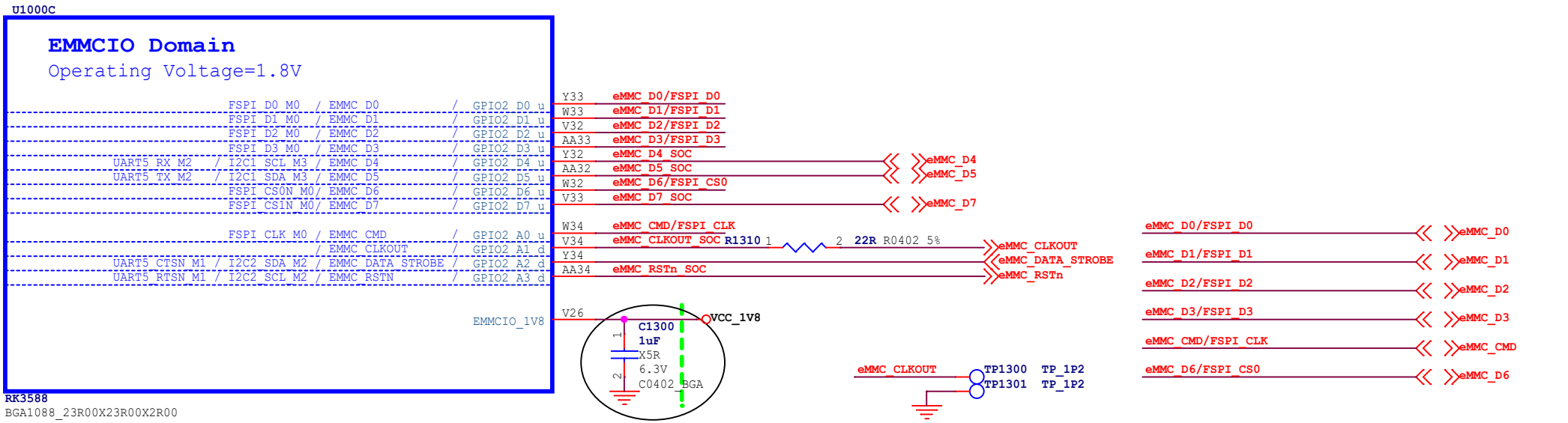






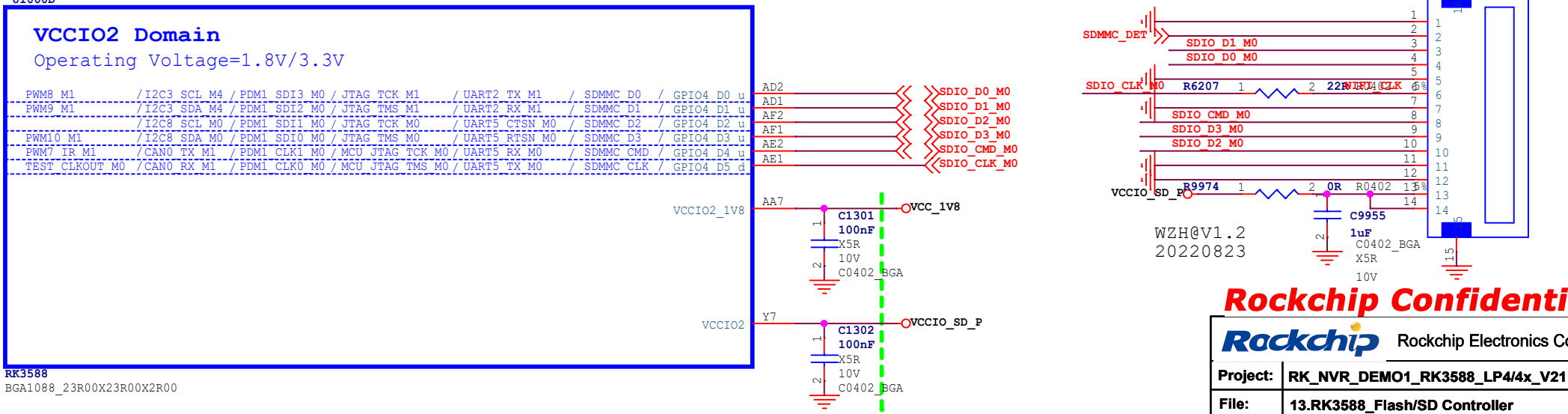
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	12.RK3588 DDR Controler				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	12 of 43

RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

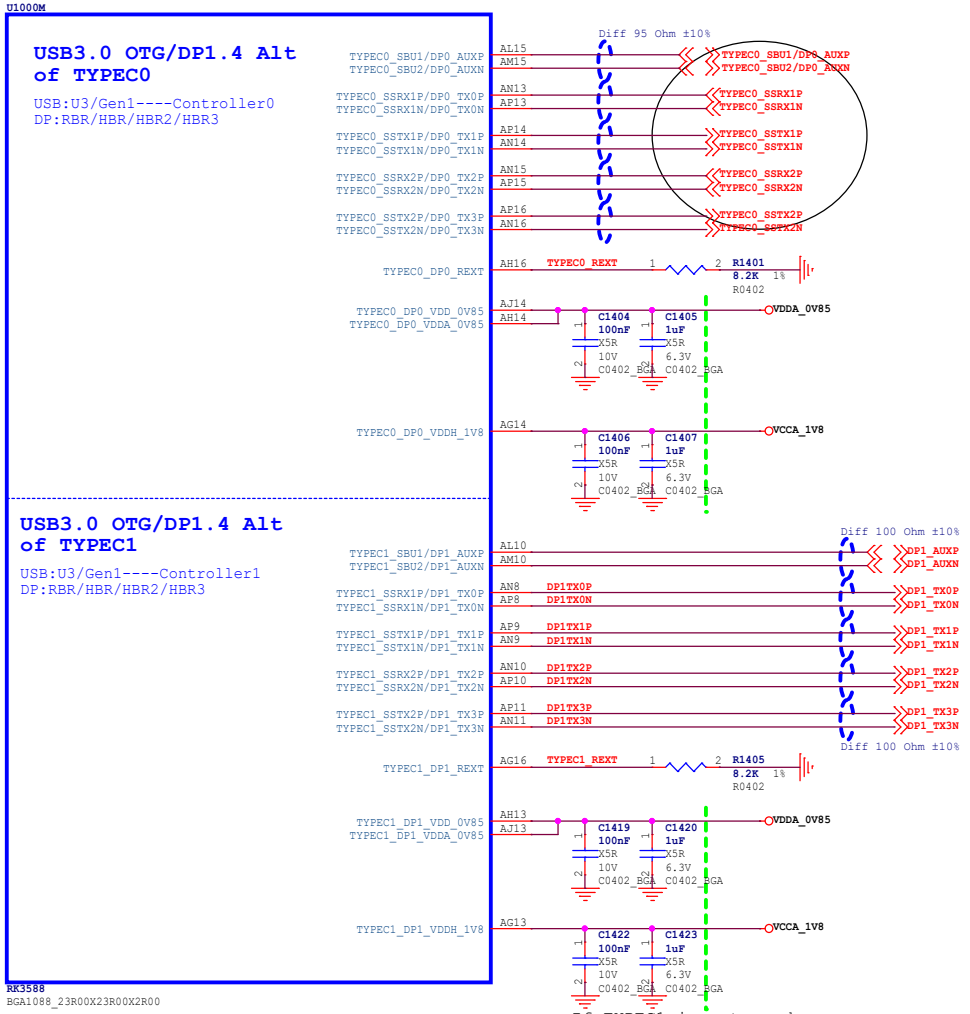


Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	13.RK3588_Flash/SD Controller		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Sheet: 13 of 43

RK3588_M(TYPEC/DP)

If TYPEC0 is not used,
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power



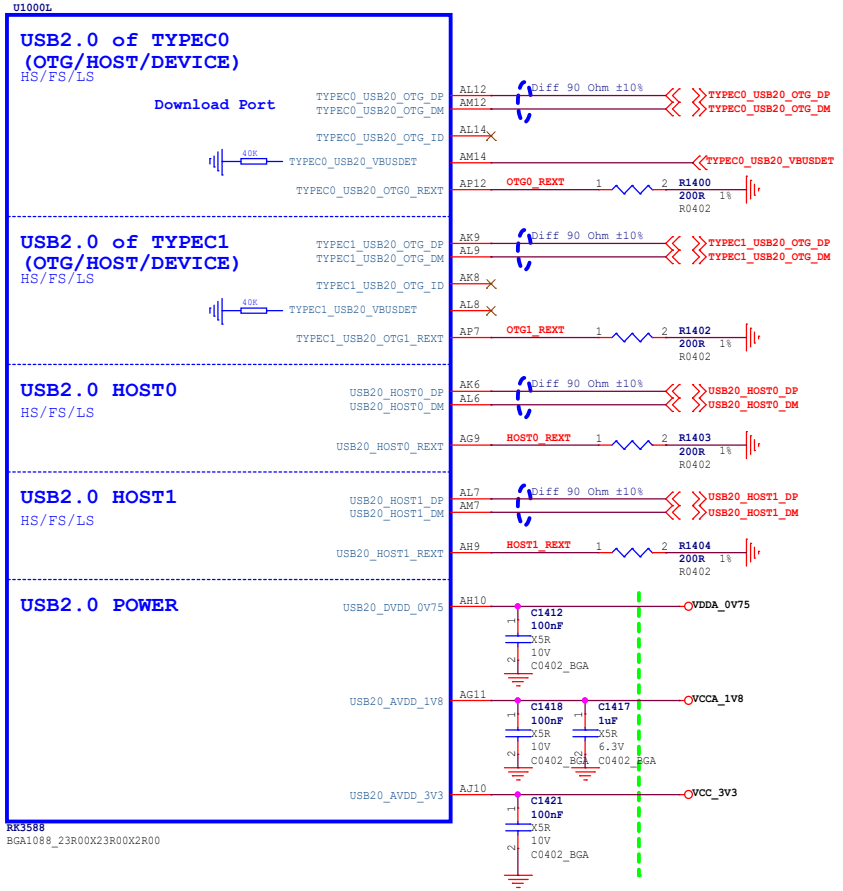
If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588_L(USB2.0 HOST/OTG)



Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:

If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:

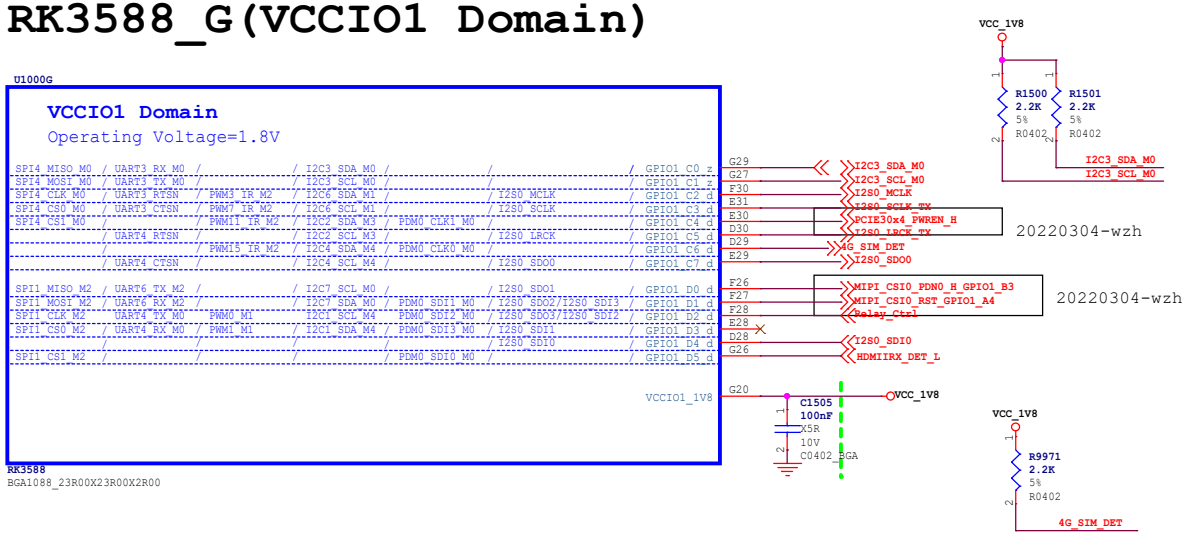
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:

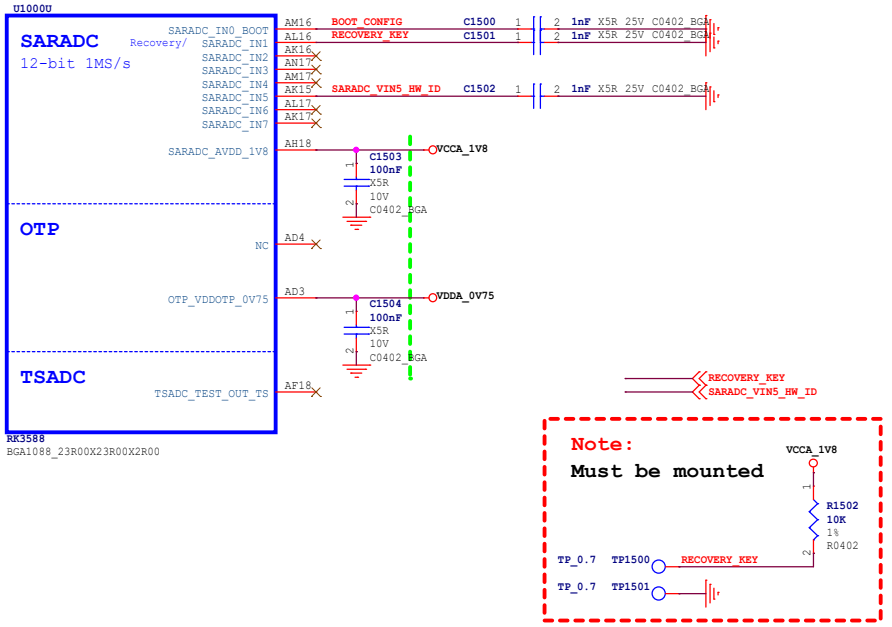
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Thursday, September 15, 2022		Rev:	V2.1	
Designed by:	Zhangdz	Reviewed by:		Sheet:	14 of 43

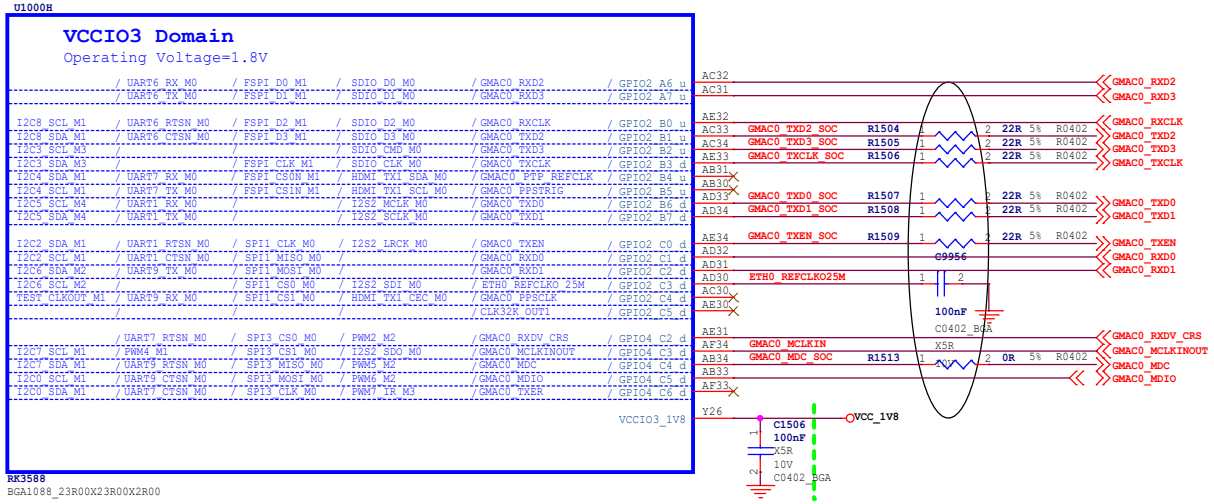
RK3588_G(VCCIO1 Domain)



RK3588_U(SARADC/OTP)

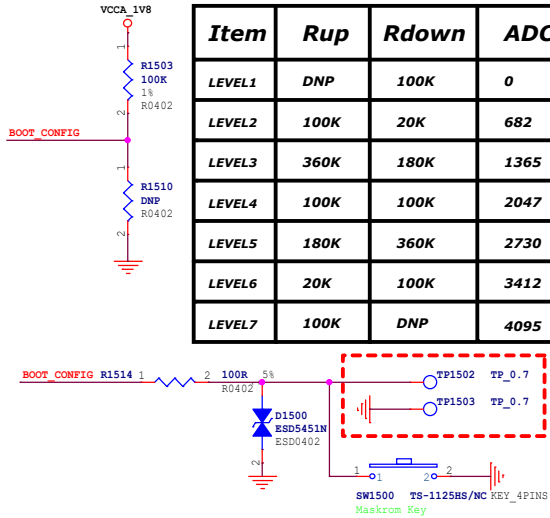


RK3588_H(VCCIO3 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

BOOT MODE CONFIG



Item	Rup	Rdown	ADC	VOL	Boot sequence
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

It is recommended to reserve this circuit to enter the MaskROM state for update firmware

Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Sheet: 15 of 43

RK3588_Q/R(MIPI_D/C_PHY0/1)

If not used,
Signal:leave floating
Power: leave floating

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	AN26
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	AP26
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	AN24
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	AP24
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	AN25
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	AP25
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	AN27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	AP27
MIPI_DPHY0_TX_D3P/NO_USE	AN28
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	AP28

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	AN32
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	AP31
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	AN29
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	AP29
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	AN30
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AP30
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AN33
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	AP32
MIPI_DPHY0_RX_D3P/NO_USE	AN34
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AP33

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG	AF20
MIPI_D/C_PHY0_VDD	AG20
MIPI_D/C_PHY0_VDD_1V2	AH20
MIPI_D/C_PHY0_VDD_1V8	AJ20

RK3588
BGA1088_23R00X23R00X2R00

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	AN20
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	AP20
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	AN18
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	AP18
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	AN19
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	AP19
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	AN21
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	AP21
MIPI_DPHY1_TX_D3P/NO_USE	AN22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	AP22

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	AL21
MIPI_DPHY1_RX_D3P/NO_USE	AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	AL22

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG	AF19
MIPI_D/C_PHY1_VDD	AG19
MIPI_D/C_PHY1_VDD_1V2	AH19
MIPI_D/C_PHY1_VDD_1V8	AJ19

RK3588
BGA1088_23R00X23R00X2R00

RK3588_P(MIPI_CSI_RX_PHY)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P	AJ33	Diff 100 Ohm ±10% → MIPI_CSI0_RX_CLK0P
MIPI_CSI0_CLK0N	AJ34	Diff 100 Ohm ±10% → MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P	AG33	Diff 100 Ohm ±10% → MIPI_CSI0_RX_D0P
MIPI_CSI0_D0N	AG34	Diff 100 Ohm ±10% → MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P	AH33	Diff 100 Ohm ±10% → MIPI_CSI0_RX_D1P
MIPI_CSI0_D1N	AH34	Diff 100 Ohm ±10% → MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P	AM33	
MIPI_CSI0_CLK1N	AM34	
MIPI_CSI0_D2P	AK33	
MIPI_CSI0_D2N	AK34	
MIPI_CSI0_D3P	AL33	
MIPI_CSI0_D3N	AL34	
MIPI_CSI0_AVCC0V75	AB25	VDDA_0V75 (C1600 1uF X5R 6.3V C0402_BGA; C1601 100nF X5R 10V C0402_BGA)
MIPI_CSI0_AVCC1V8	AB26	VCCA1V8_IMAGE (C1602 1uF X5R 6.3V C0402_BGA)

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P	AJ31	Diff 100 Ohm ±10%
MIPI_CSI1_CLK0N	AJ32	
MIPI_CSI1_D0P	AG31	Diff 100 Ohm ±10%
MIPI_CSI1_D0N	AG32	
MIPI_CSI1_D1P	AH31	Diff 100 Ohm ±10%
MIPI_CSI1_D1N	AH32	
MIPI_CSI1_CLK1P	AM31	Diff 100 Ohm ±10%
MIPI_CSI1_CLK1N	AM32	
MIPI_CSI1_D2P	AK31	Diff 100 Ohm ±10%
MIPI_CSI1_D2N	AK32	
MIPI_CSI1_D3P	AL31	Diff 100 Ohm ±10%
MIPI_CSI1_D3N	AL32	
MIPI_CSI1_AVCC0V75	AA25	VDDA_0V75 (C1604 1uF X5R 6.3V C0402_BGA) → Power merging, capacitance sharing
MIPI_CSI1_AVCC1V8	AA26	VCCA1V8_IMAGE (C1603 100nF X5R 10V C0402_BGA) → Power merging, capacitance sharing

RK3588
BGA1088_23R00X23R00X2R00

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:

When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21			
File:	16.RK3588_MIPI Interface			
Date:	Thursday, September 15, 2022		Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Sheet	16 of 43

RK3588_S(HDMI2.1 TX)

If not used,
Signal:leave floating
Power: Tie to VSS

U1000S

HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_SBDP/EDP_TX0_AUXP (AG2)
HDMI_TX0_SBDN/EDP_TX0_AUXN (AG1)
HDMI_TX0_D0P/EDP_TX0_D0P (AJ2)
HDMI_TX0_D0N/EDP_TX0_D0N (AJ1)
HDMI_TX0_D1P/EDP_TX0_D1P (AK3)
HDMI_TX0_D1N/EDP_TX0_D1N (AK2)
HDMI_TX0_D2P/EDP_TX0_D2P (AL2)
HDMI_TX0_D2N/EDP_TX0_D2N (AL1)
HDMI_TX0_D3P/EDP_TX0_D3P (AH3)
HDMI_TX0_D3N/EDP_TX0_D3N (AH2)
HDMI/EDP_TX0_REXT (AM2) HDMI_TX0_REXT — R1708 8.2K 1% R0402
HDMI/EDP_TX0_VDD_0V75 (AA9) <260mA — C1709 4.7uF X5R 6.3V C0402_BGA; C1710 4.7uF X5R 10V C0603 — VDDA0V75_IMAGE
HDMI/EDP_TX0_AVDD_0V75 (AB9) <1mA — C1711 1uF X5R 6.3V C0402_BGA
HDMI/EDP_TX0_VDD_IO_1V8 (AC7)
HDMI/EDP_TX0_VDD_CMN_1V8 (AC6) — C1713 1uF X5R 6.3V C0402_BGA; C1714 100nF X5R 10V C0402_BGA; C1715 4.7uF X5R 6.3V C0402_BGA — VCCA1V8_IMAGE

Note:
Close to HDMI Connector

HDMI0_TX0P_PORT/eDP0_TX_D0P — C1700 220nF C0201 X5R 10V
HDMI0_TX0N_PORT/eDP0_TX_D0N — C1701 220nF C0201 X5R 10V
HDMI0_TX1P_PORT/eDP0_TX_D1P — C1702 220nF C0201 X5R 10V
HDMI0_TX1N_PORT/eDP0_TX_D1N — C1703 220nF C0201 X5R 10V
HDMI0_TX2P_PORT/eDP0_TX_D2P — C1704 220nF C0201 X5R 10V
HDMI0_TX2N_PORT/eDP0_TX_D2N — C1705 220nF C0201 X5R 10V
HDMI0_TX3P_PORT/eDP0_TX_D3P — C1706 220nF C0201 X5R 10V
HDMI0_TX3N_PORT/eDP0_TX_D3N — C1707 220nF C0201 X5R 10V

Diff 100 Ohm ±10%

HDMI0_TX0P_PORT
HDMI0_TX0N_PORT
HDMI0_TX1P_PORT
HDMI0_TX1N_PORT
HDMI0_TX2P_PORT
HDMI0_TX2N_PORT
HDMI0_TX3P_PORT
HDMI0_TX3N_PORT

Note:
Close to HDMI Connector

R1700 499R 1% R0201; R1701 499R 1% R0201; R1702 499R 1% R0201; R1703 499R 1% R0201; R1704 499R 1% R0201; R1705 499R 1% R0201; R1706 499R 1% R0201; R1707 499R 1% R0201

HDMI0_TX_ON_H — Q1700 WNM6002-3/TR SOT_323; Q1701 WNM6002-3/TR SOT_323; Q1702 WNM6002-3/TR SOT_323; Q1703 WNM6002-3/TR SOT_323

Note:

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX1_SBDP/EDP_TX1_AUXP (AN2)
HDMI_TX1_SBDN/EDP_TX1_AUXN (AP2)
HDMI_TX1_D0P/EDP_TX1_D0P (AN4)
HDMI_TX1_D0N/EDP_TX1_D0N (AP4)
HDMI_TX1_D1P/EDP_TX1_D1P (AM5)
HDMI_TX1_D1N/EDP_TX1_D1N (AN5)
HDMI_TX1_D2P/EDP_TX1_D2P (AN6)
HDMI_TX1_D2N/EDP_TX1_D2N (AP6)
HDMI_TX1_D3P/EDP_TX1_D3P (AM3)
HDMI_TX1_D3N/EDP_TX1_D3N (AN3)
HDMI/EDP_TX1_REXT (AN1)
HDMI/EDP_TX1_VDD_0V75 (AD9)
HDMI/EDP_TX1_AVDD_0V75 (AC9)
HDMI/EDP_TX1_VDD_IO_1V8 (AD7)
HDMI/EDP_TX1_VDD_CMN_1V8 (AD6)

RK3588
BGA1088_23R00X23R00X2R00

U1000T

HDMI RX

HDMI:V2.0

HDMI_RX_D0P (AG5) / HDMI_RX_D0N (AG4) — HDMI_RX_D0P / HDMI_RX_D0N
HDMI_RX_D1P (AH6) / HDMI_RX_D1N (AH5) — HDMI_RX_D1P / HDMI_RX_D1N
HDMI_RX_D2P (AJ5) / HDMI_RX_D2N (AJ4) — HDMI_RX_D2P / HDMI_RX_D2N
HDMI_RX_CLKP (AF6) / HDMI_RX_CLKN (AF5) — HDMI_RX_CLKP / HDMI_RX_CLKN
HDMI_RX_REXT (AF3) HDMI_RX_REXT — R1730 200R R0402 1%
HDMI_RX_AVDD0V75 (AE8) — C1738 1uF X5R 6.3V C0402 — <40mA — VDDA0V75_IMAGE
HDMI_RX_VPH3V3 (AE4) — <80mA — VCCA_3V3_P
HDMI_RX_DVDD3V3 (AE5) — C1740 100nF X5R 6.3V C0402; C1741 1uF X5R 6.3V C0402

RK3588
BGA1088_23R00X23R00X2R00

HDMI20_RX
100 Ohm +-10%

RK3588_T(HDMI20 RX)

If not used,
Signal:leave floating
Power: leave floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	17.RK3588_HDMI/eDP Interface		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by: Zhangdz	Reviewed by:	Sheet:	17 of 43

RK3588_N(PCIE20)

If not used,
Signal:leave floating
Power: Tie to VSS

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN — L32 / L33 — Diff 100 Ohm ±10%
PCIE20_0_TXP/SATA30_0_TXP — M34 — SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN — M33 — SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP — N33 — SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN — N34 — SATA30_0_RXN
PCIE20_SATA30_0_AVDD_0V85 — M28 — VDDA_0V85 — C1801 10uF X5R 4V C0402_BGA
PCIE20_SATA30_0_AVDD_1V8 — M27 — VCCA_1V8 — C1803 4.7uF X5R 6.3V C0402_BGA

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN — H32 / H33 — Diff 100 Ohm ±10%
PCIE20_1_TXP/SATA30_1_TXP — K33 — PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN — K34 — PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP — J33 — PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN — J34 — PCIE20_1_RXN/SATA30_1_RXN
PCIE20_SATA30_1_AVDD_0V85 — L28 — VDDA_0V85 — C1808 100nF X5R 10V C0402_BGA
PCIE20_SATA30_1_AVDD_1V8 — L27 — VCCA_1V8 — C1810 100nF X5R 10V C0402_BGA

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN — G31 / G30 — Diff 90 Ohm ±10%
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP — H30 — USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H29 — USB30_2_SSTXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP — J31 — USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J30 — USB30_2_SSRXN
PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — VDDA_0V85 — C1816 1uF X5R 6.3V C0402_BGA
PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — VCCA_1V8 — C1819 4.7uF X5R 6.3V C0402_BGA

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

Power merging, capacitance sharing

RK3588
BGA1088_23R00X23R00X2R00

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3588_O(PCIE30)

Note:
Only PCIE30 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input

Lane0
PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN — E33 / E34 — Diff 100 Ohm ±10% — PCIE30_PORT0_REFCLKP_IN / PCIE30_PORT0_REFCLKN_IN
PCIE30_PORT0_TX0P — D32 — Diff 85 Ohm ±10% — PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N — D33 — PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P — G33 — Diff 85 Ohm ±10% — PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N — G34 — PCIE30_PORT0_RX0N

Lane1
PCIE30_PORT0_TX1P — C33 — Diff 85 Ohm ±10% — PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N — C34 — PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P — F32 — Diff 85 Ohm ±10% — PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N — F33 — PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1800 200R 1% R0402
PCIE30_PORT0_AVDD0V75 — G24 — VDDA_0V75 — C1804 1uF X5R 6.3V C0402_BGA — C1805 4.7uF X5R 6.3V C0402_BGA
PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8 — C1806 1uF X5R 6.3V C0402_BGA — C1807 4.7uF X5R 6.3V C0402_BGA

PCIE30 PORT1

input

Lane0
PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN — A28 / B28 — Diff 100 Ohm ±10% — PCIE30_PORT1_REFCLKP_IN / PCIE30_PORT1_REFCLKN_IN
PCIE30_PORT1_TX0P — B30 — Diff 85 Ohm ±10% — PCIE30_PORT1_TX2P
PCIE30_PORT1_TX0N — A30 — PCIE30_PORT1_TX2N
PCIE30_PORT1_RX0P — B32 — Diff 85 Ohm ±10% — PCIE30_PORT1_RX2P
PCIE30_PORT1_RX0N — A32 — PCIE30_PORT1_RX2N

Lane1
PCIE30_PORT1_TX1P — C29 — Diff 85 Ohm ±10% — PCIE30_PORT1_TX3P
PCIE30_PORT1_TX1N — B29 — PCIE30_PORT1_TX3N
PCIE30_PORT1_RX1P — C31 — Diff 85 Ohm ±10% — PCIE30_PORT1_RX3P
PCIE30_PORT1_RX1N — B31 — PCIE30_PORT1_RX3N

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1801 200R 1% R0402
PCIE30_PORT1_AVDD0V75 — H24 — VDDA_0V75 — C1812 1uF X5R 6.3V C0402_BGA — C1813 4.7uF X5R 6.3V C0402_BGA
PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8 — C1814 100nF X5R 10V C0402_BGA — C1815 4.7uF X5R 6.3V C0402_BGA

RK3588
BGA1088_23R00X23R00X2R00

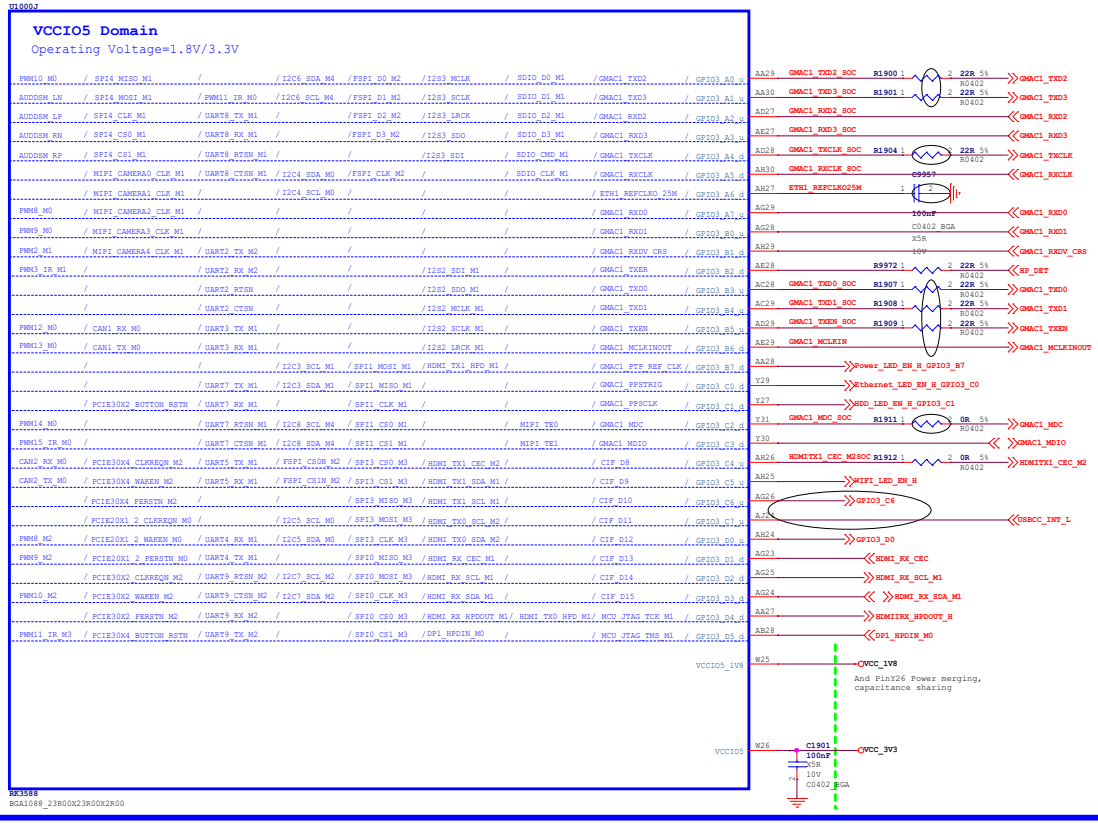
Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

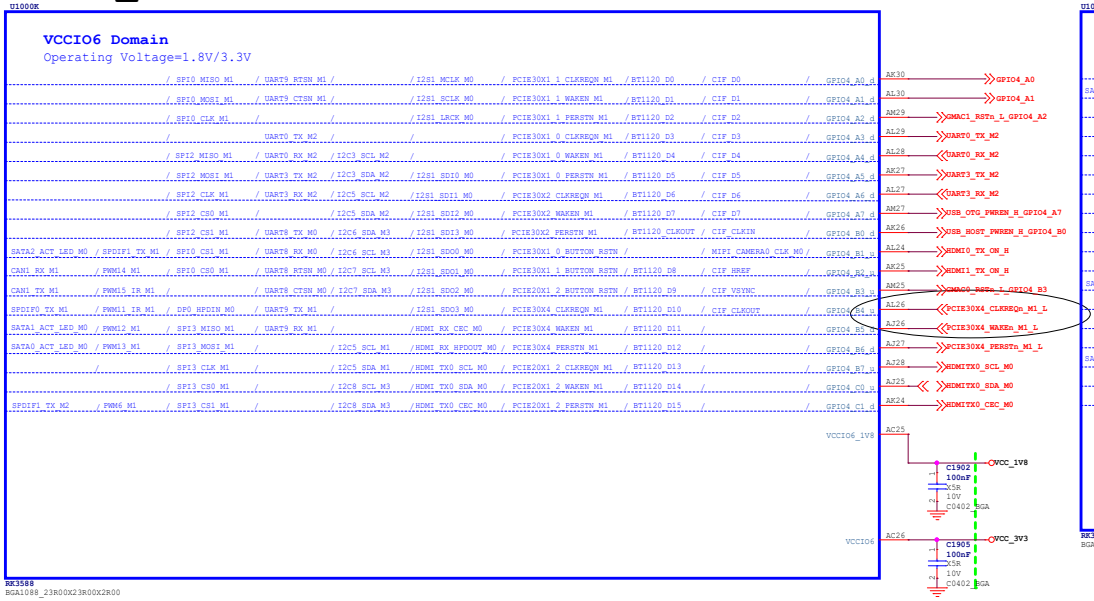
If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
Date:	Thursday, September 15, 2022		Rev:	V2.1	
Designed by:	Zhangdz	Reviewed by:		Sheet:	18 of 43

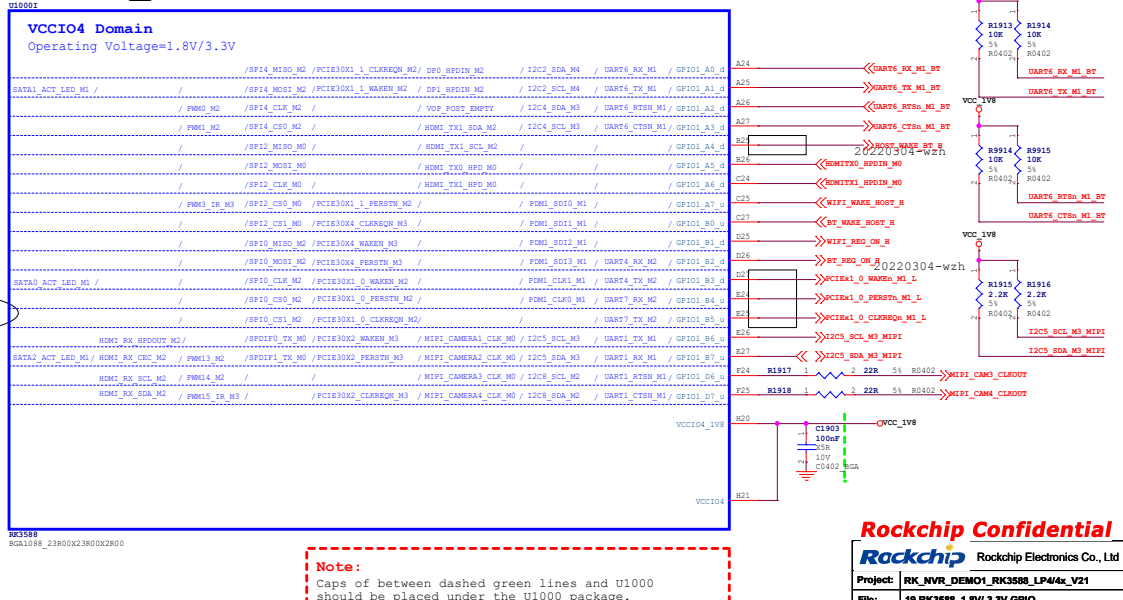
RK3588_J(VCCIO5 Domain)



RK3588_K(VCCIO6 Domain)



RK3588_I(VCCIO4 Domain)



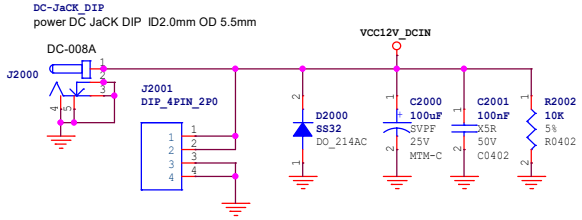
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

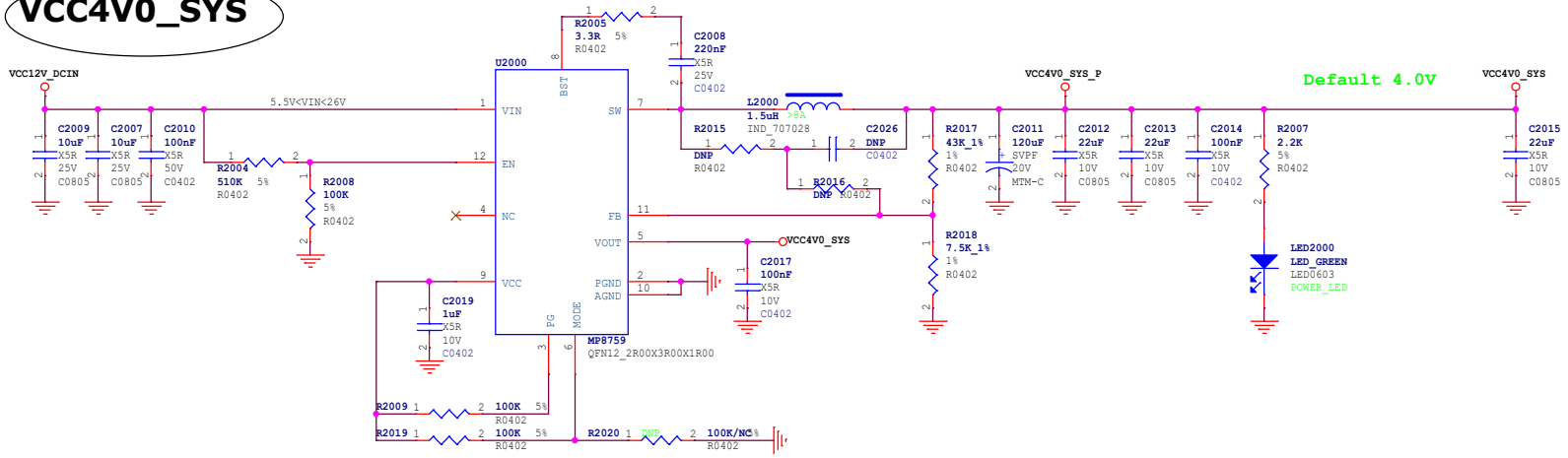
Rockchip Electronics Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	19.RK3588_1.8V/ 3.3V GPIO		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by: Zhangdz	Reviewed by:	Sheet:	19 of 43

12V/3A DCIN

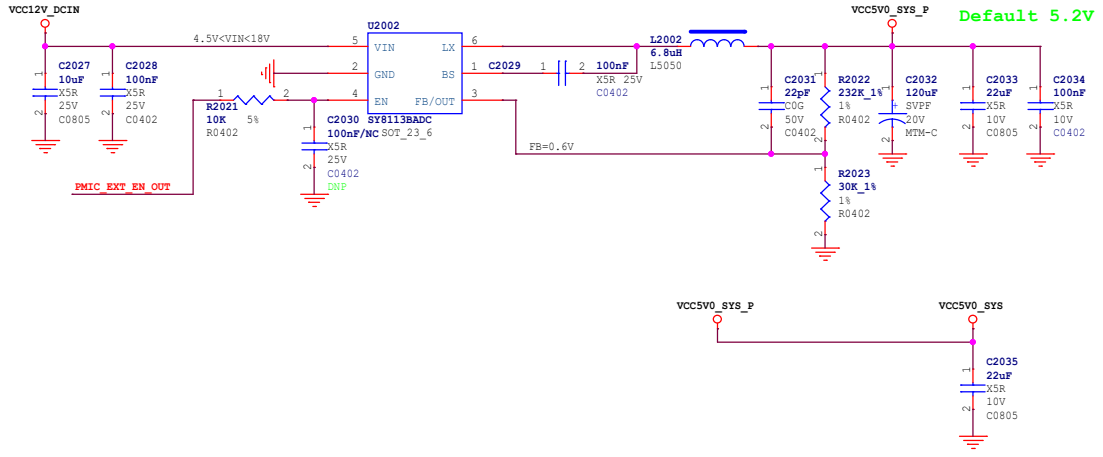
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe



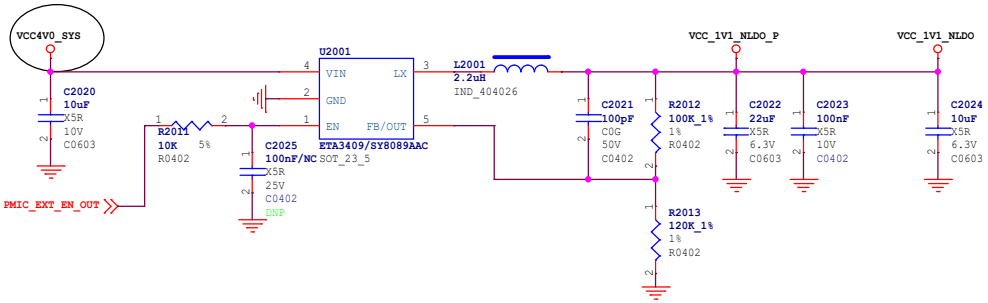
VCC4V0_SYS



VCC5V0_SYS



VCC_1V1_NLDO



Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	20.Power_DC IN				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 43

PMIC RK806-1 BUCK

PMIC_SPI_CS
PMIC_SPI_MOSI
PMIC_SPI_CLK
PMIC_PWR_CTRL1
PMIC_PWR_CTRL2
PMIC_PWR_CTRL3
PMIC_INT_L
RESET_L
PMIC_EXT_EN_OUT

U2200A

BUCK5 2.5A / BUCK1 6.5A
BUCK6 2.5A / BUCK2 5A
BUCK9 2.5A / BUCK3 5A
BUCK8 2.5A / BUCK4 5A
BUCK10 2.5A / BUCK7 2.5A

RK806-1
QFN68_7R00X7R00X0R80_T

Default:0.85V
Low frequency:
0.85V-->0.75V

VDD_DDR
Feedback from RK3588

Default:1.1V

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

Default 0 ohm.
If need end feedback,
need change to 100ohm
Reserved for end feedback

Default:0.6V

VDDQ_DDR
Feedback from RK3588

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

Default:3.3V

Default:1.8V

Default:2.0V

VDD_GPU
VDD_CPU_LIT
VDD_LOGIC
VDD_VDENC
Feedback from RK3588

DCDC
OUT
FB
VDD
RK3588

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

ED2200 AZ5825-01F ESD0402

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25~6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

PMIC RK806-1 Managerment

U2200C

VCCIO
VCCA

Default:1.8V

PMIC_SPI_CS
PMIC_SPI_MOSI
PMIC_SPI_CLK
PMIC_PWR_CTRL3
PMIC_PWR_CTRL2
PMIC_PWR_CTRL1
PMIC_EXT_EN_OUT
PMIC_INT_L
RESET_L

PMIC_VDC
PWRON_L

RK806-1
QFN68_7R00X7R00X0R80_T

RK3588 nPOR
TSADC_SHUT
RK806-1 RESETB
Reset Key

Note:
Reset Key Control Path
TSADC_SHUT Control Path
RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

PLDO
NLDO

Default:1.8V
Default:1.2V
Default:3.3V
Default:0.75V
Default:0.85V;Low frequency:0.85V-->0.75V
Default:0.85V

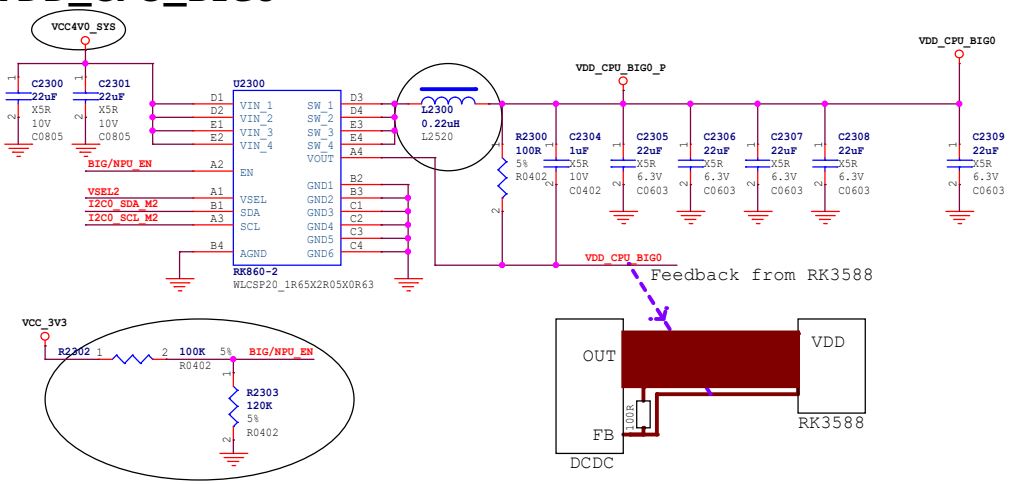
Note:

The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

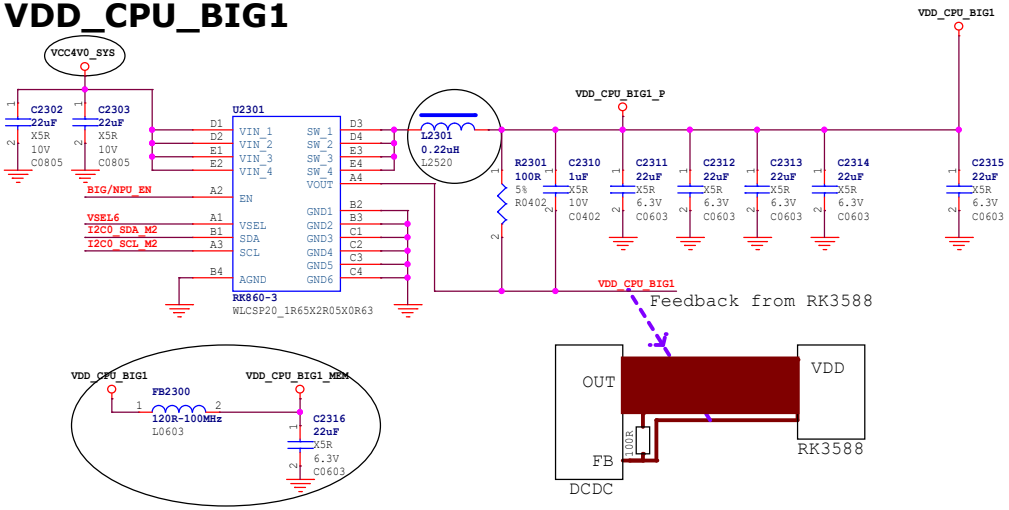
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	22.Power-PMIC_RK806-1		
Date:	Thursday, September 15, 2022	Rev:	V2.1
Designed by: Zhangtz	Reviewed by: Default	Sheet:	21 of 43

RTCIC_INT_L_GPIO0_B2
VSEL2
VSEL3
VSEL6
BIG
NPU
BIG
I2C2_SCL_M0
I2C2_SDA_M0
I2C0_SCL_M2
I2C0_SDA_M2
I2C6_SDA_M0
I2C6_SCL_M0

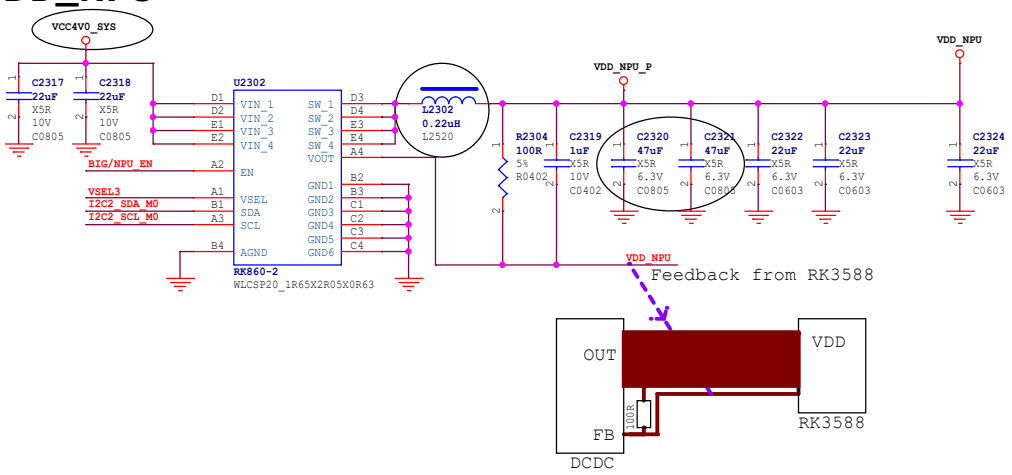
VDD_CPU_BIG0



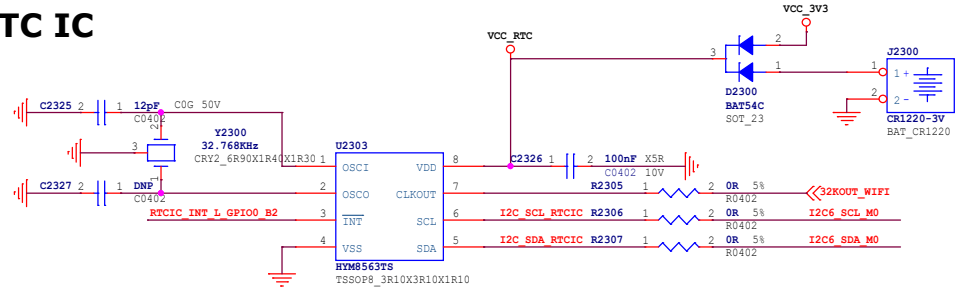
VDD_CPU_BIG1



VDD_NPU



RTC IC

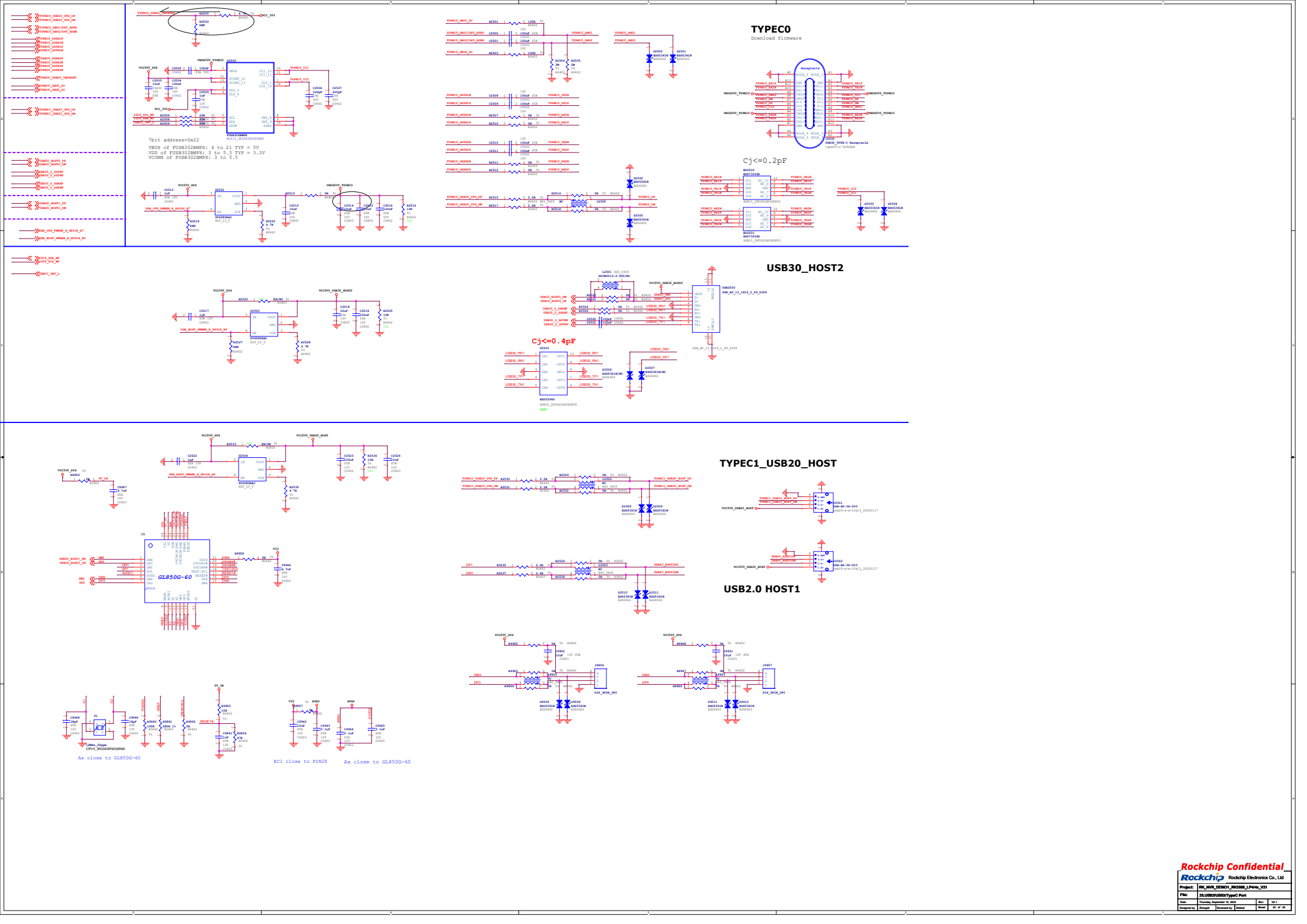


Address:Read A3H,Write A2H

Rockchip Confidential

Rockchip Electronics Co., Ltd

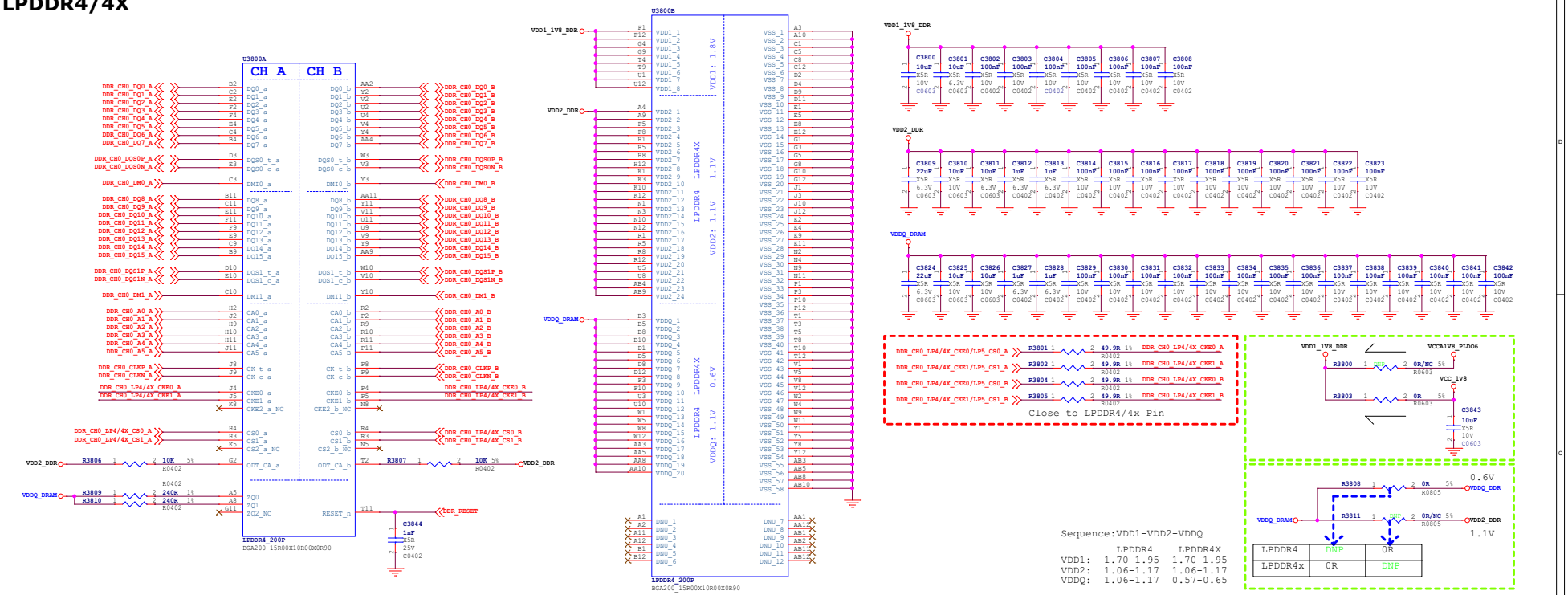
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	23.Power_Ext Discrete/RTC IC				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 43



Rockchip Confidential

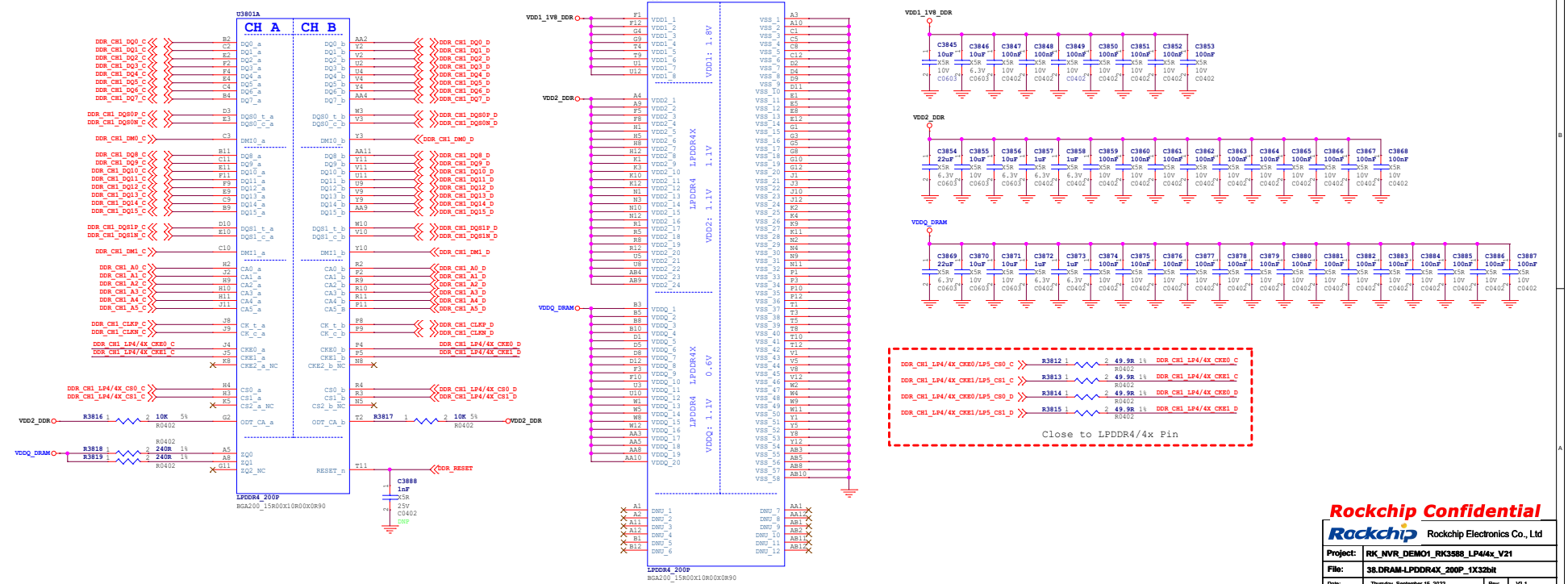
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	26.USB2/3/USB3/TypeC Port
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangjh
Reviewed by:	Default
Sheet:	23 of 45

LPDDR4/4X



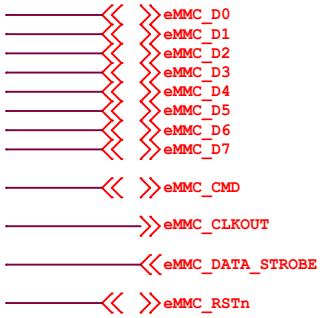
Sequence:VDD1-VDD2-VDDQ

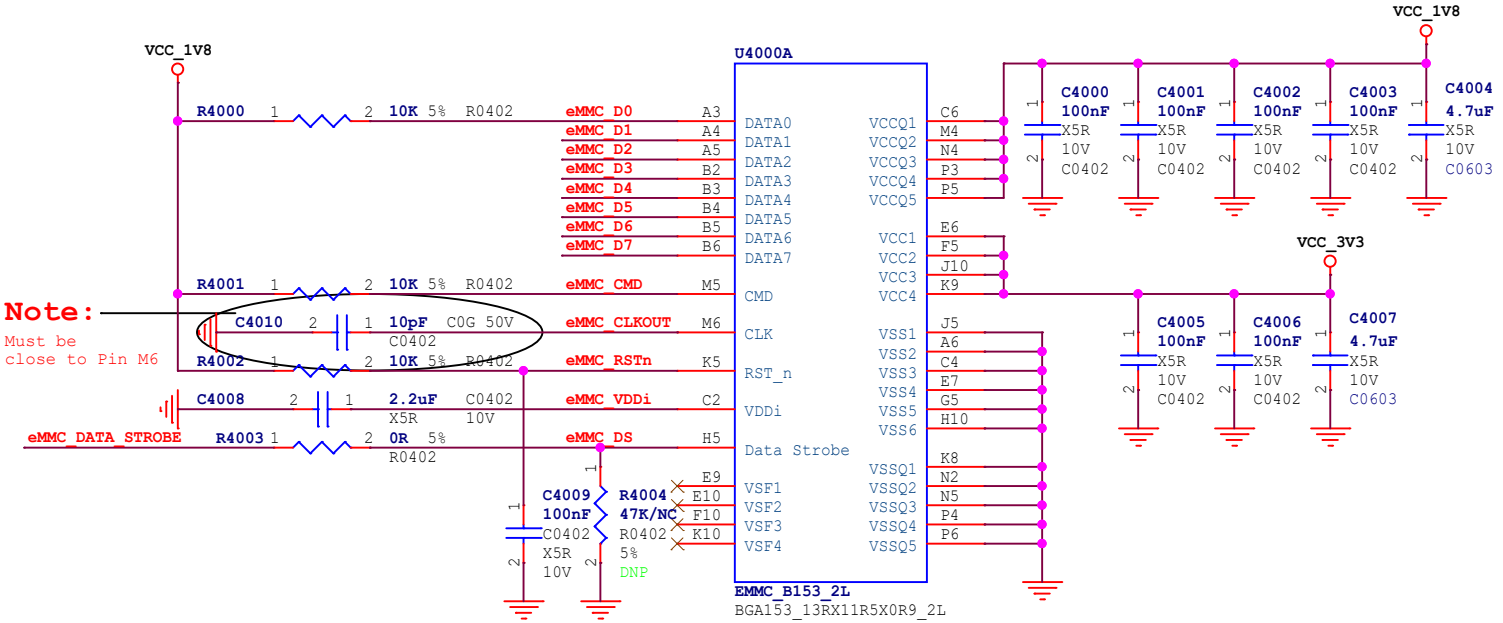
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

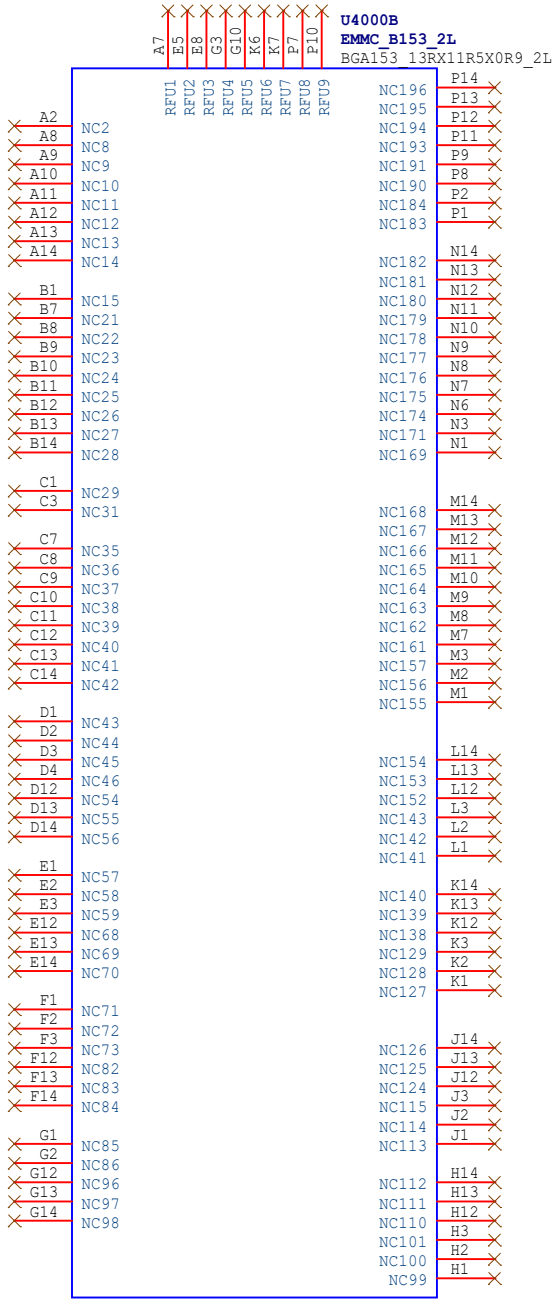


Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	38.DRAM-LPDDR4X_200P_1X32bit
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangdz
Reviewed by:	
Sheet:	24 of 43

eMMC Flash







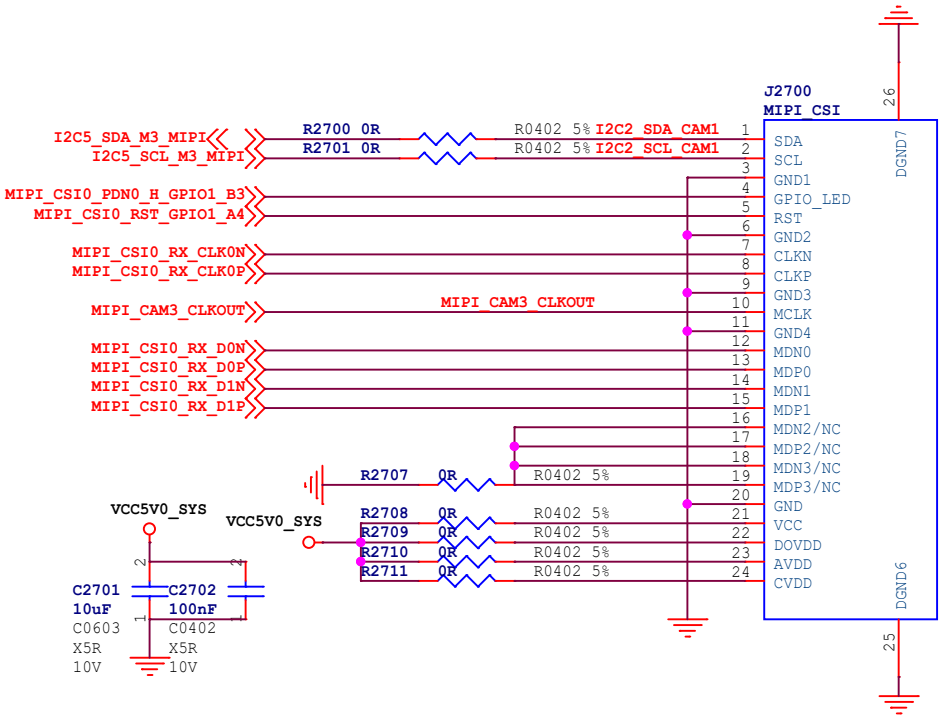
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	40.Flash-eMMC Flash				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	25 of 43

SPI Flash

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	43.Flash-SPI FLASH(Option)				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	26 of 43

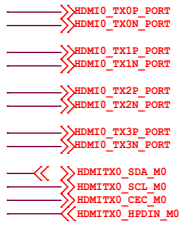
MIPI-CSI0_RX



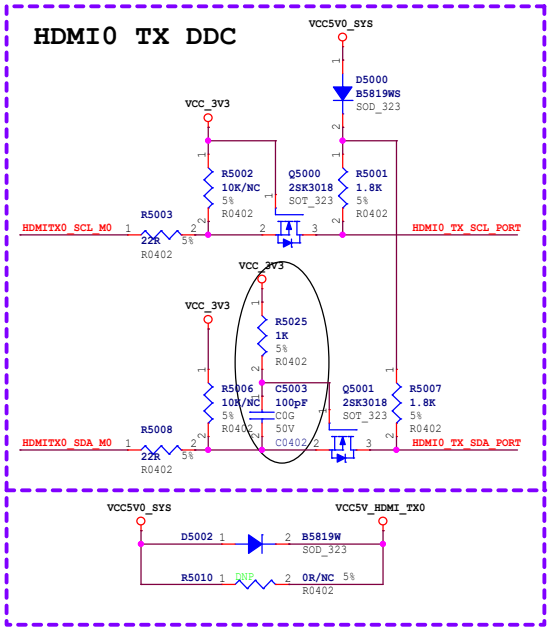
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	47.VI-Camera_MIPI-CSI				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	27 of 43

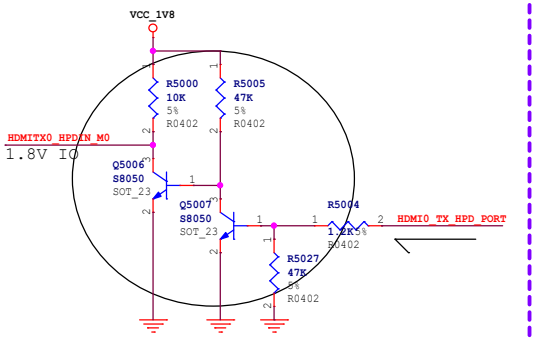
HDMI TX0



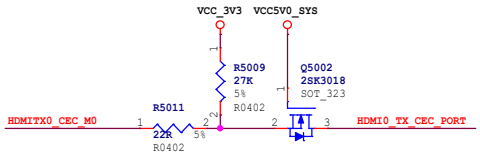
HDMI0 TX DDC

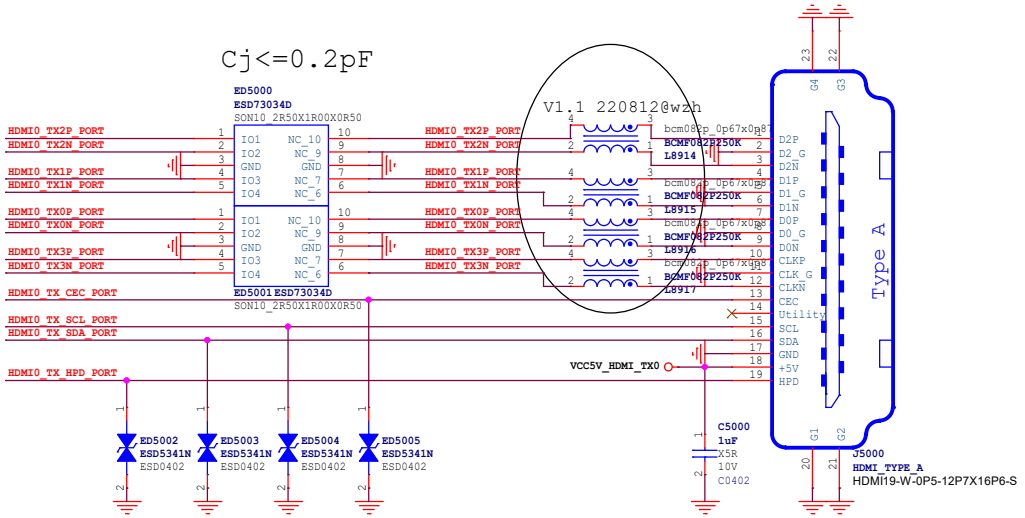


HDMI0 TX HPD



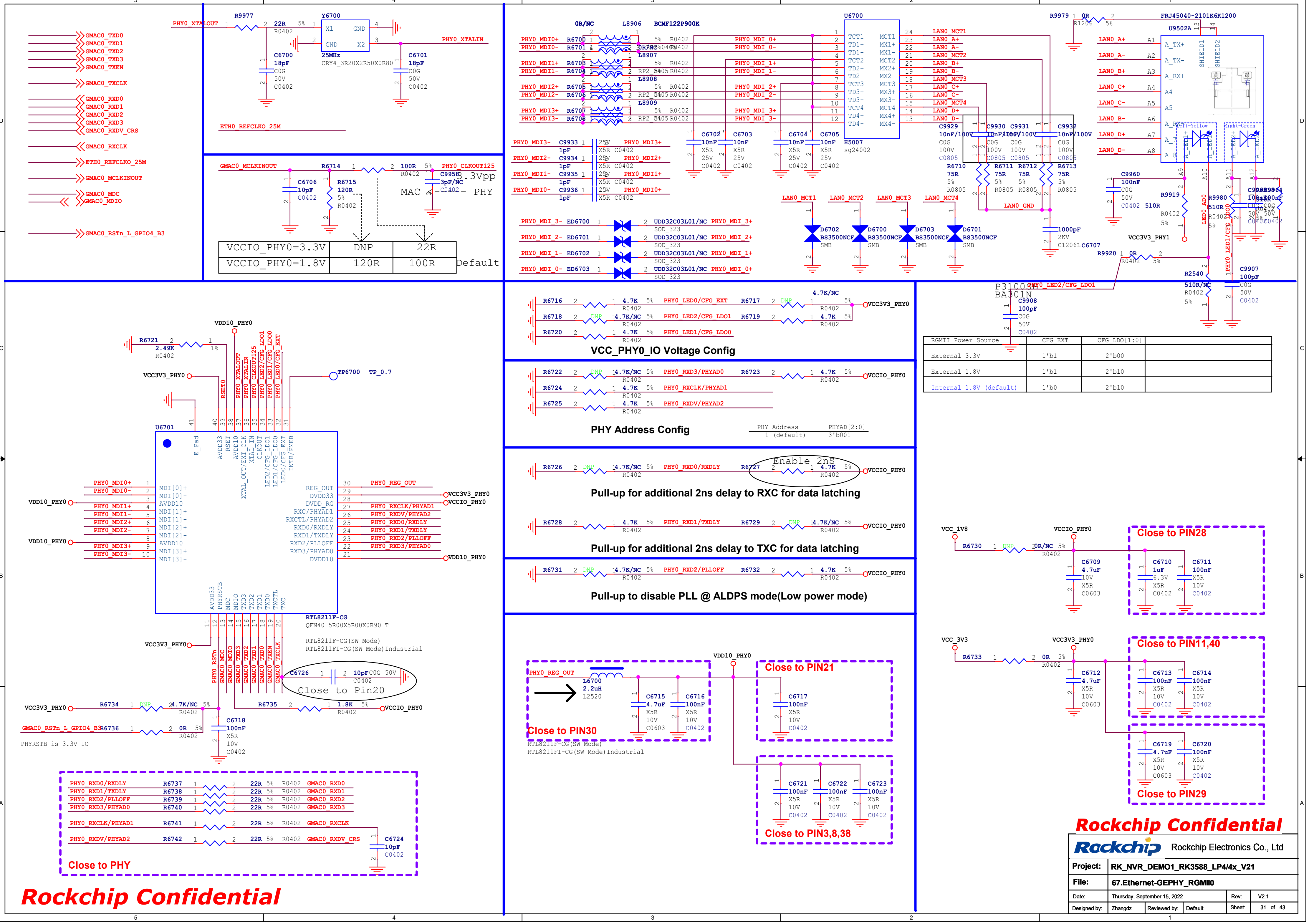
HDMI0 TX CEC





Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	50.VO-HDMI2.1 TX				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:		Sheet:	28 of 43



VCCIO_PHY0=3.3V	DNP	22R
VCCIO_PHY0=1.8V	120R	100R

Default

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V (default)	1'b0	2'b10

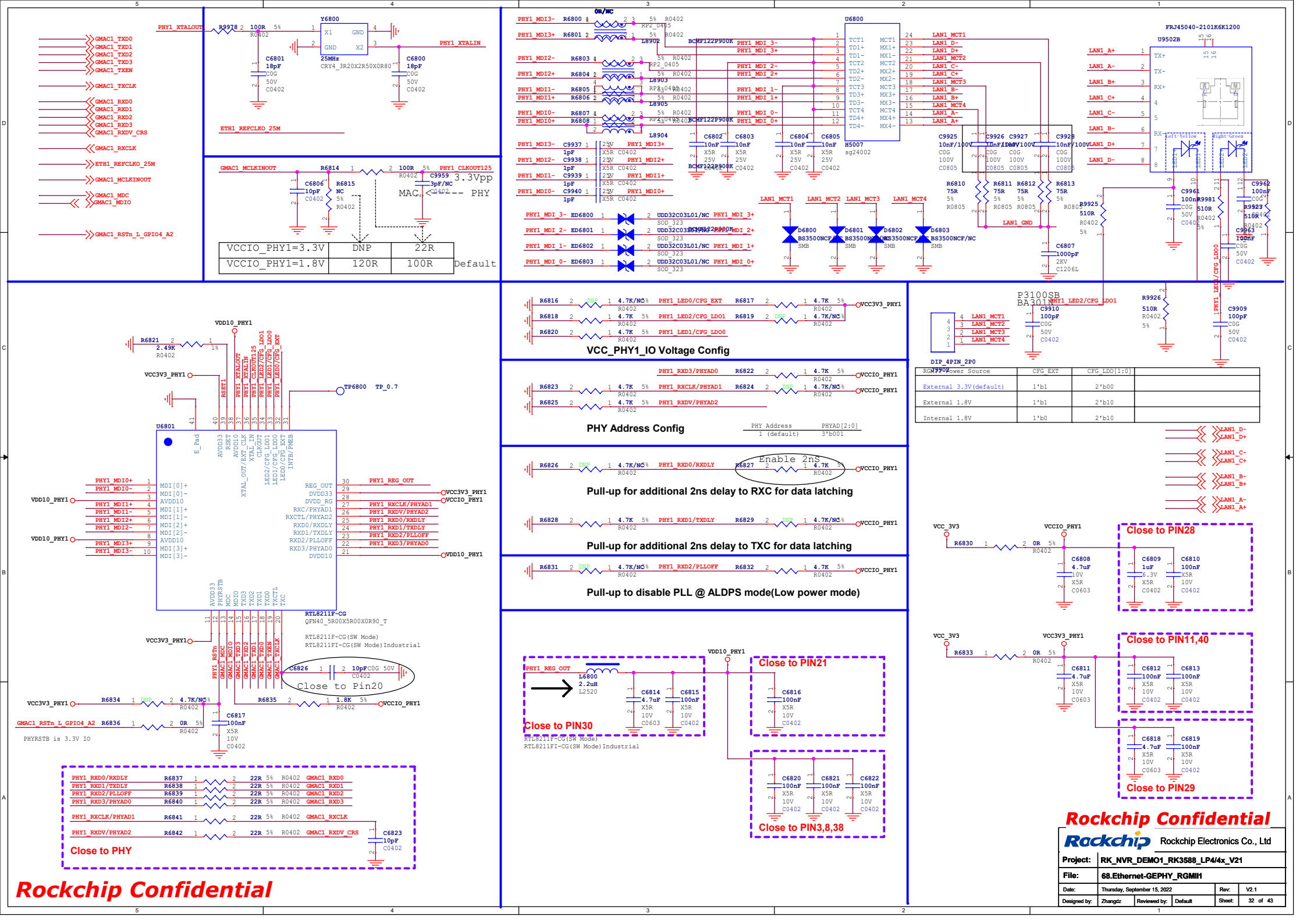
PHY Address	PHYAD[2:0]
1 (default)	3'b001

Rockchip Confidential

Rockchip Electronics Co., Ltd

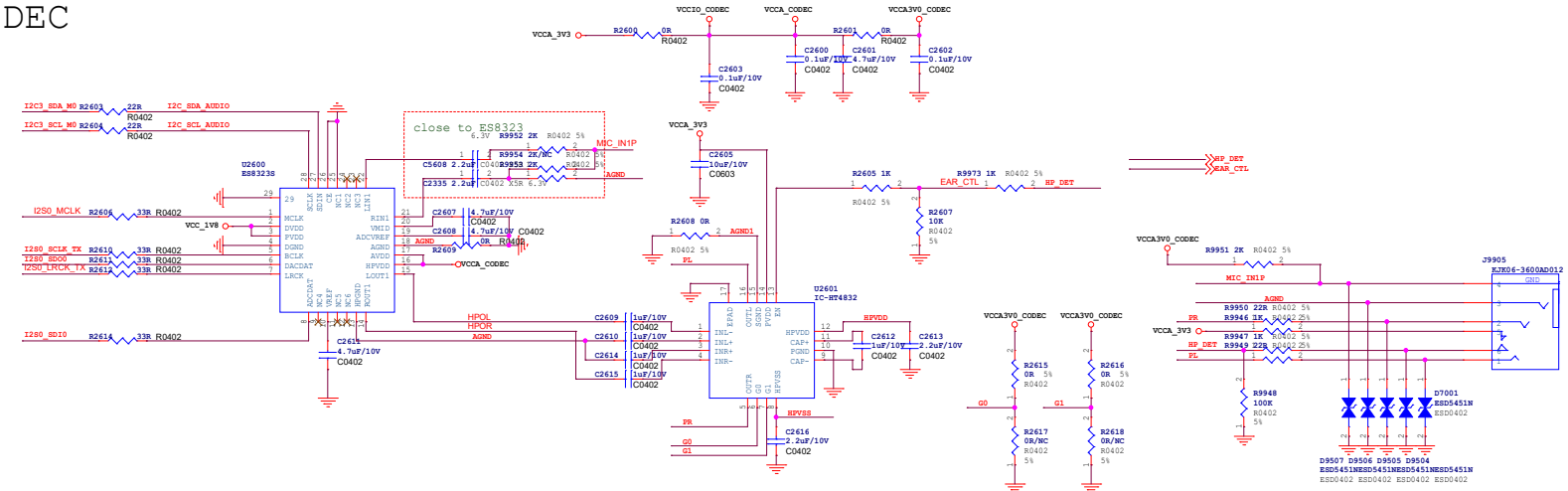
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	67.Ethernet-GEPHY_RGMII0
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangdz
Reviewed by:	Default
Sheet:	31 of 43

Rockchip Confidential


GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS
GMAC1_RXCLK
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO
GMAC1_RSTn_L_GPIO4_A2
PHY1_XTALOUT
R9978 100R 5% R0402
Y6800
X1 GND GND X2
25MHz
CRY4_3R20X2R50X0R80
PHY1_XTALIN
C6801 18pF C0G 50V C0402
C6800 18pF C0G 50V C0402
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
R6814 1 2 100R 5% R0402
PHY1_CLKOUT125
C6806 10pF C0402
R6815 NC 5% R0402
C9959 3pF/NC C0402
3.3Vpp
MAC <-- PHY
VCCIO_PHY1=3.3V DNP 22R
VCCIO_PHY1=1.8V 120R 100R Default
PHY1_MDI3- R6800 1 2 0R/NC 5% R0402
PHY1_MDI3+ R6801 2 3 5% R0402
RP2_0405
L8902
PHY1_MDI2- R6803 1 2 3 5% R0402
PHY1_MDI2+ R6804 2 3 5% R0402
RP2_0405
L8903
PHY1_MDI1- R6805 1 2 3 5% R0402
PHY1_MDI1+ R6806 2 3 5% R0402
RP2_0405
L8905
PHY1_MDI0- R6807 1 2 3 5% R0402
PHY1_MDI0+ R6808 2 3 5% R0402
RP2_0405
L8904
BCMF122P900K
U6800
TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-
LAN1_MCT1 LAN1_D- LAN1_D+ LAN1_MCT2 LAN1_C- LAN1_C+ LAN1_MCT3 LAN1_B- LAN1_B+ LAN1_MCT4 LAN1_A- LAN1_A+
H5007 sg24002
FRJ45040-2101K6K1200
U9502B
TX+ TX- RX+ RX-
LAN1_A+ LAN1_A- LAN1_B+ LAN1_C+ LAN1_C- LAN1_B- LAN1_D+ LAN1_D-
Left-Yellow
Right-Green
C9925 10nF/100V C0G 100V C0805
C9926 C9927 10nF/100V C0G 100V C0805
C9928 10nF/100V C0G 100V C0805
R6810 75R 5% R0805
R6811 R6812 75R 5% R0805
R6813 75R 5% R0805
LAN1_GND
C6807 1000pF 2KV C1206L
C9961 100nF C0G 50V C0402
R9981 510R R0402 5%
R9925 510R R0402 5%
C9962 100nF C0G 50V C0402
R9923 510R R0402 5%
C9963 100nF C0G 50V C0402
PHY1_MDI3- C9937 1pF 25V X5R C0402 PHY1_MDI3+
PHY1_MDI2- C9938 1pF 25V X5R C0402 PHY1_MDI2+
PHY1_MDI1- C9939 1pF 25V X5R C0402 PHY1_MDI1+
PHY1_MDI0- C9940 1pF 25V X5R C0402 PHY1_MDI0+
C6802 10nF X5R 25V C0402
C6803 10nF X5R 25V C0402
C6804 10nF X5R 25V C0402
C6805 10nF X5R 25V C0402
PHY1_MDI_3- ED6800 1 2 UDD32C03L01/NC PHY1_MDI_3+ SOD_323
PHY1_MDI_2- ED6801 1 2 UDD32C03L01/NC PHY1_MDI_2+ SOD_323
PHY1_MDI_1- ED6802 1 2 UDD32C03L01/NC PHY1_MDI_1+ SOD_323
PHY1_MDI_0- ED6803 1 2 UDD32C03L01/NC PHY1_MDI_0+ SOD_323
LAN1_MCT1 LAN1_MCT2 LAN1_MCT3 LAN1_MCT4
D6800 BS3500NCF/NC SMB
D6801 BS3500NCF/NC SMB
D6802 BS3500NCF/NC SMB
D6803 BS3500NCF/NC SMB
VDD10_PHY1
R6821 2.49K 1% R0402
VCC3V3_PHY1
TP6800 TP_0.7
U6801
E_Pad
AVDD33 RSET AVDD10 XTAL_OUT/EXT_CLK XTAL_IN CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB
PHY1_XTALOUT PHY1_XTALIN PHY1_CLKOUT125 PHY1_LED2/CFG_LDO1 PHY1_LED1/CFG_LDO0 PHY1_LED0/CFG_EXT
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
PHY1_MDI0+ PHY1_MDI0- PHY1_MDI1+ PHY1_MDI1- PHY1_MDI2+ PHY1_MDI2- PHY1_MDI3+ PHY1_MDI3-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY1_REG_OUT PHY1_RXCLK/PHYAD1 PHY1_RXDV/PHYAD2 PHY1_RXD0/RXDLY PHY1_RXD1/TXDLY PHY1_RXD2/PLLOFF PHY1_RXD3/PHYAD0
VCC3V3_PHY1 VCCIO_PHY1 VDD10_PHY1
AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
PHY1_RSTn GMAC1_MDC GMAC1_MDIO GMAC1_TXD3 GMAC1_TXD2 GMAC1_TXD1 GMAC1_TXD0 GMAC1_TXEN GMAC1_TXCLK
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C6826 1 2 10pF C0G 50V C0402
Close to Pin20
R6834 1 DNP 2 4.7K/NC 5% R0402
R6835 2 1 1.8K 5% R0402
VCCIO_PHY1
C6817 100nF X5R 10V C0402
GMAC1_RSTn_L_GPIO4_A2 R6836 1 2 0R 5% R0402
PHYRSTB is 3.3V IO
PHY1_RXD0/RXDLY R6837 1 2 22R 5% R0402 GMAC1_RXD0
PHY1_RXD1/TXDLY R6838 1 2 22R 5% R0402 GMAC1_RXD1
PHY1_RXD2/PLLOFF R6839 1 2 22R 5% R0402 GMAC1_RXD2
PHY1_RXD3/PHYAD0 R6840 1 2 22R 5% R0402 GMAC1_RXD3
PHY1_RXCLK/PHYAD1 R6841 1 2 22R 5% R0402 GMAC1_RXCLK
PHY1_RXDV/PHYAD2 R6842 1 2 22R 5% R0402 GMAC1_RXDV_CRS
C6823 10pF C0402
Close to PHY
R6816 2 DNP 1 4.7K/NC 5% R0402 PHY1_LED0/CFG_EXT
R6817 2 1 4.7K 5% R0402 VCC3V3_PHY1
R6818 2 1 4.7K 5% R0402 PHY1_LED2/CFG_LDO1
R6819 2 DNP 1 4.7K/NC 5% R0402
R6820 2 1 4.7K 5% R0402 PHY1_LED1/CFG_LDO0
VCC_PHY1_IO Voltage Config
R6823 2 1 4.7K 5% R0402 PHY1_RXCLK/PHYAD1
R6824 2 DNP 1 4.7K/NC 5% R0402 VCCIO_PHY1
R6825 2 1 4.7K 5% R0402 PHY1_RXDV/PHYAD2
PHY Address Config
PHY Address 1 (default)
PHYAD[2:0] 3'b001
R6826 2 DNP 1 4.7K/NC 5% R0402 PHY1_RXD0/RXDLY
R6827 2 1 4.7K 5% R0402 VCCIO_PHY1
Enable 2ns
Pull-up for additional 2ns delay to RXC for data latching
R6828 2 1 4.7K 5% R0402 PHY1_RXD1/TXDLY
R6829 2 DNP 1 4.7K/NC 5% R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to TXC for data latching
R6831 2 DNP 1 4.7K/NC 5% R0402 PHY1_RXD2/PLLOFF
R6832 2 1 4.7K 5% R0402 VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
VDD10_PHY1
PHY1_REG_OUT
L6800 2.2uH L2520
C6814 4.7uF X5R 10V C0603
C6815 100nF X5R 10V C0402
Close to PIN30
C6816 100nF X5R 10V C0402
Close to PIN21
C6820 100nF X5R 10V C0402
C6821 100nF X5R 10V C0402
C6822 100nF X5R 10V C0402
Close to PIN3,8,38
P3100SB
BA301
PHY1_LED2/CFG_LDO1
R9926 510R R0402 5%
C9909 100pF C0G 50V C0402
C9910 100pF C0G 50V C0402
DIP_4PIN_2P0
J9902
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V(default) | 1'b1 | 2'b00
External 1.8V | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
LAN1_D- LAN1_D+ LAN1_C- LAN1_C+ LAN1_B- LAN1_B+ LAN1_A- LAN1_A+
VCC_3V3
VCCIO_PHY1
R6830 1 2 0R 5% R0402
C6808 4.7uF 10V X5R C0603
C6809 1uF 6.3V X5R C0402
C6810 100nF X5R 10V C0402
Close to PIN28
VCC_3V3
VCC3V3_PHY1
R6833 1 2 0R 5% R0402
C6811 4.7uF X5R 10V C0603
C6812 100nF X5R 10V C0402
C6813 100nF X5R 10V C0402
Close to PIN11,40
C6818 4.7uF X5R 10V C0603
C6819 100nF X5R 10V C0402
Close to PIN29
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_NVR_DEMO1_RK3588_LP4/4x_V21
File: 68.Ethernet-GEPHY_RGMII
Date: Thursday, September 15, 2022
Rev: V2.1
Designed by: Zhangdz
Reviewed by: Default
Sheet: 32 of 43
Rockchip Confidential

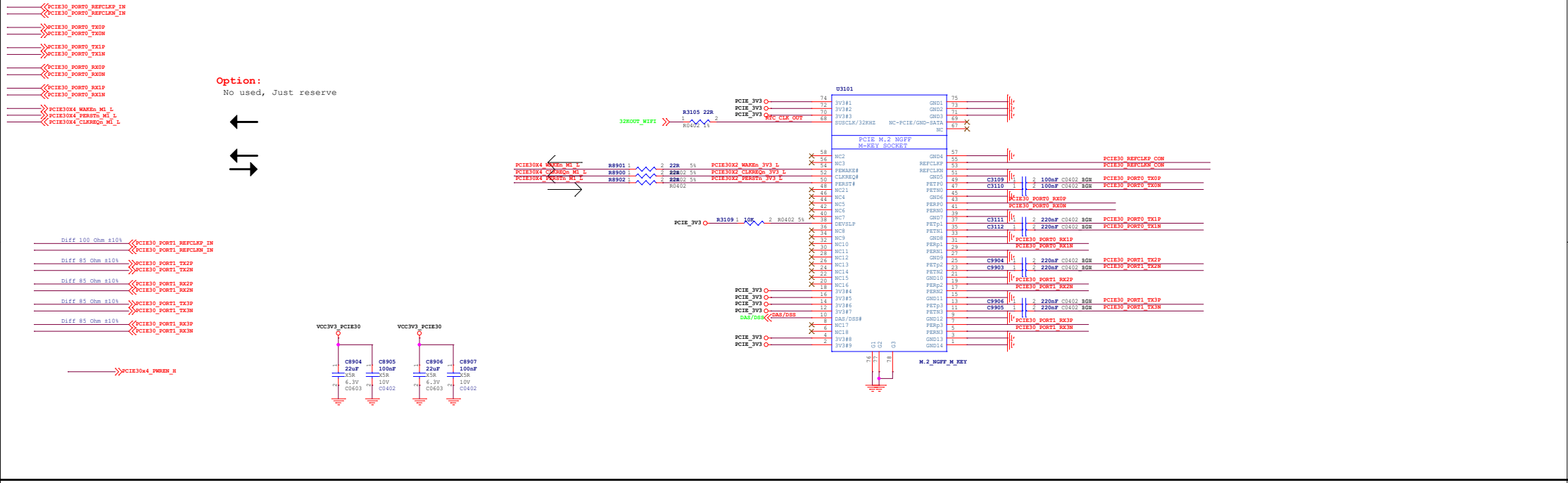
I2S0_MCLK
I2S0_SCLK_TX
I2S0_LRCK_TX
I2S0_SDO0
I2S0_SDI0
I2C3_SDA_M0
I2C3_SCL_M0

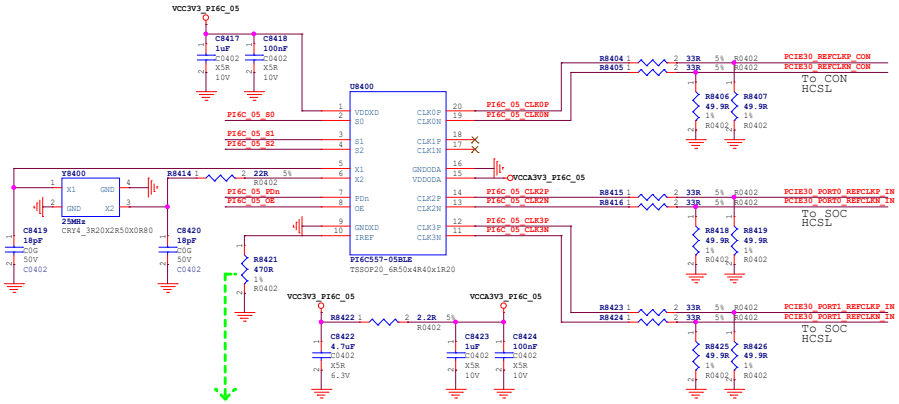
CODEC



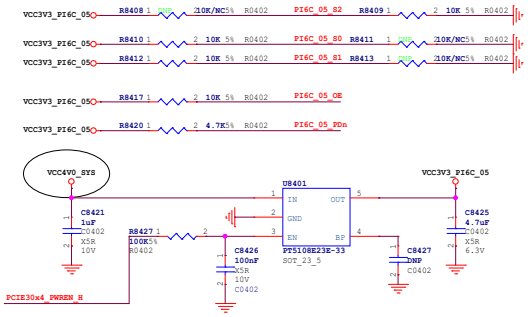
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	70.Audio Port
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	33 of 43

M.2_PCIe3.0 x 2Lanes



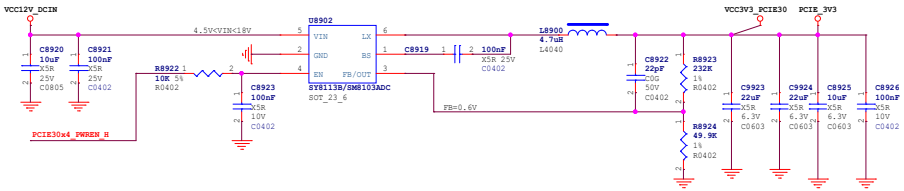


PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq
0	0	0	-0.5	100MHz
0	0	1	-1.0	100MHz
0	1	0	-1.5	100MHz
0	1	1	No Spread	100MHz



M.2 Power

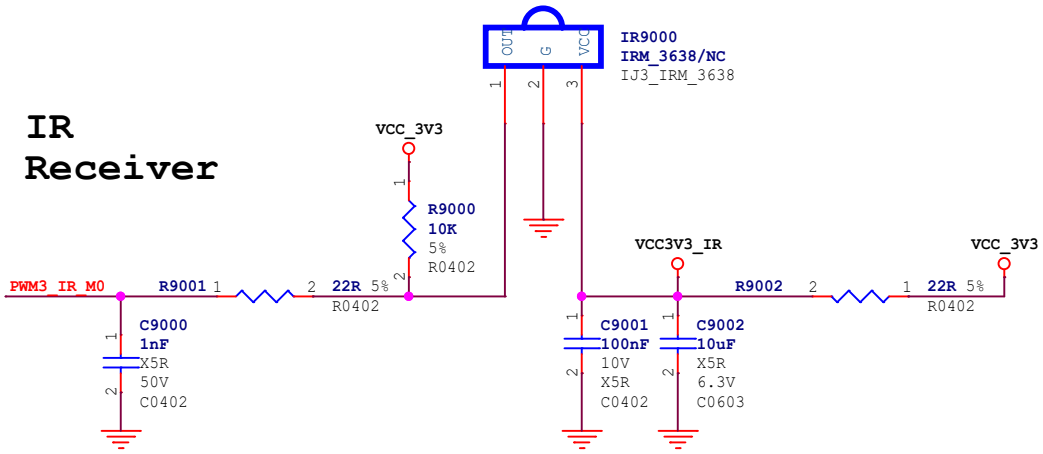
Default 3.39V



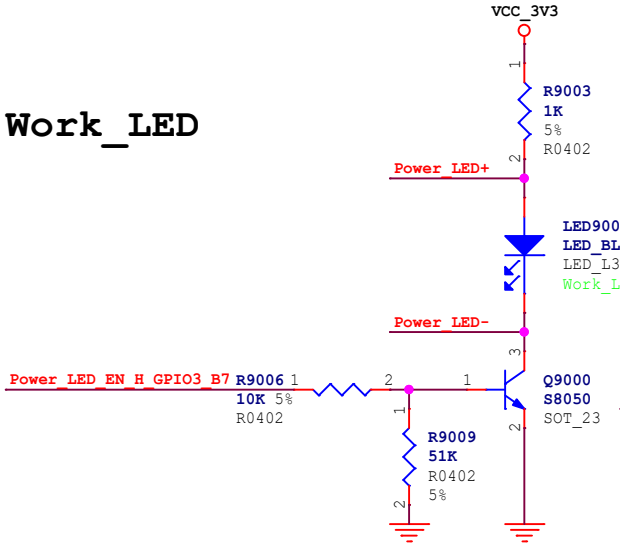
Rockchip	Rockchip Electronics Co., Ltd
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21
File:	89.M.2-PCIE3.0_1x4Lanes
Date:	Thursday, September 15, 2022
Rev:	V2.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	36 of 43

PWM3_IR_M0
Power_LED_EN_H_GPIO3_B7
Ethernet_LED_EN_H_GPIO3_C0
HDD_LED_EN_H_GPIO3_C1
Power_LED-
WIFI_LED_EN_H
4G_LED

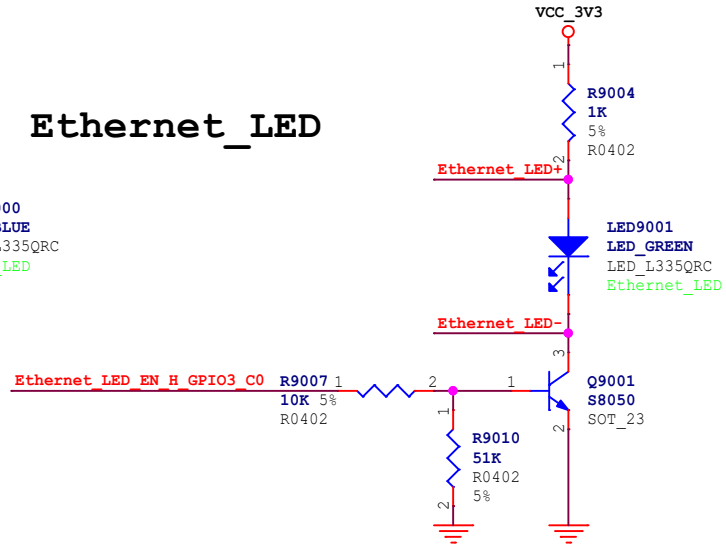
IR Receiver

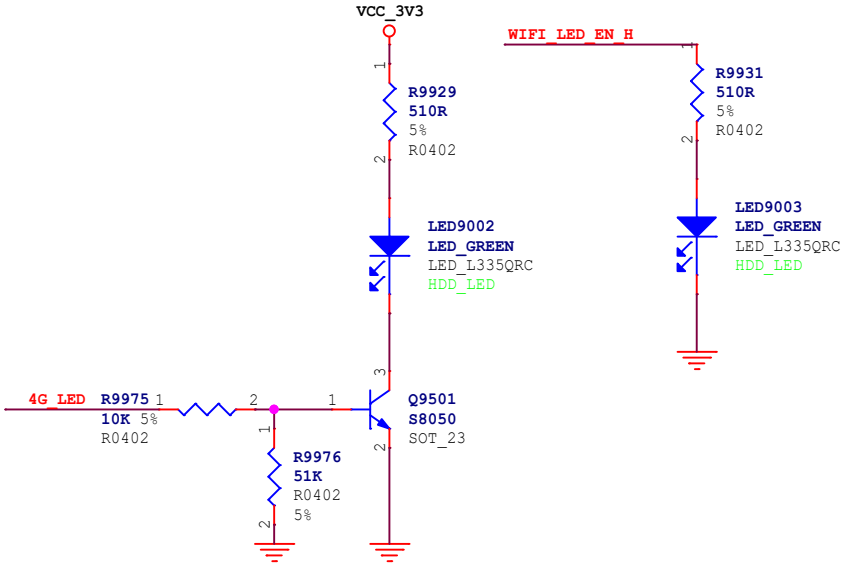


Work_LED



Ethernet_LED





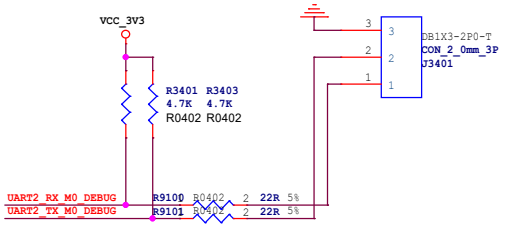
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	90.IR Receiver/LED				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	37 of 43

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2

Option1



Rockchip Confidential

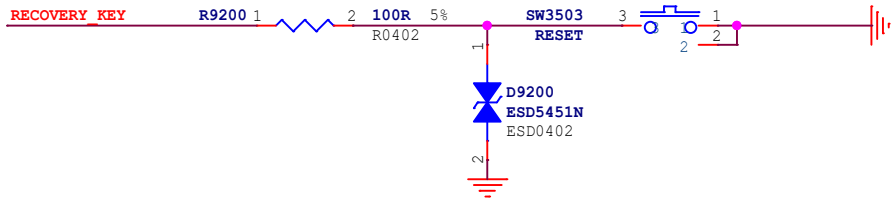
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	91.Debug UART/JTAG				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	38 of 43

RECOVERY_KEY

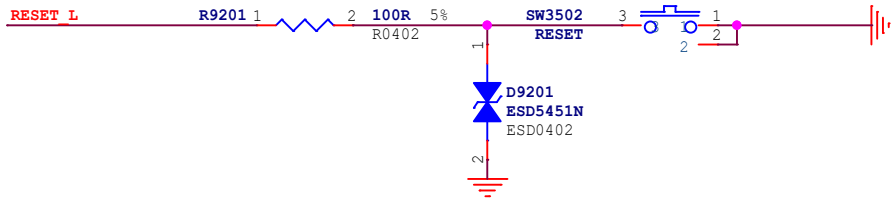
RESET_L

RECOVERY_Key

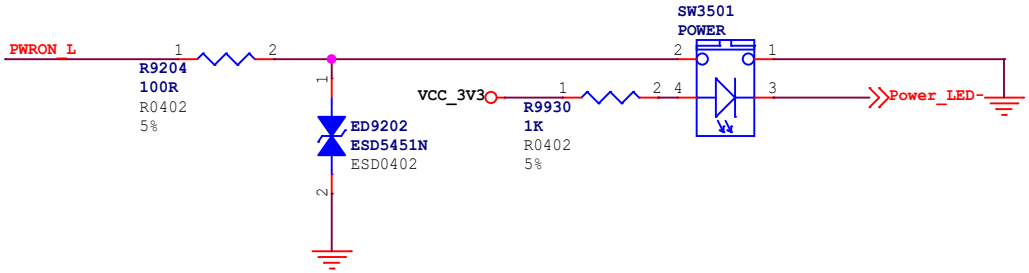
It is recommended to keep the circuit for the actual product update firmware



Reset_Key



PWRON_L

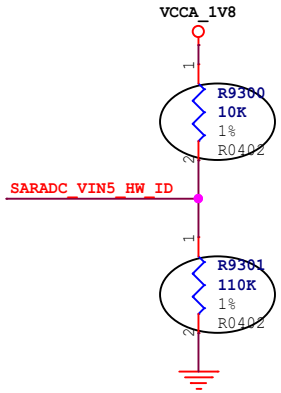


Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	92.KEY				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	39 of 43

SARADC_VIN5_HW_ID

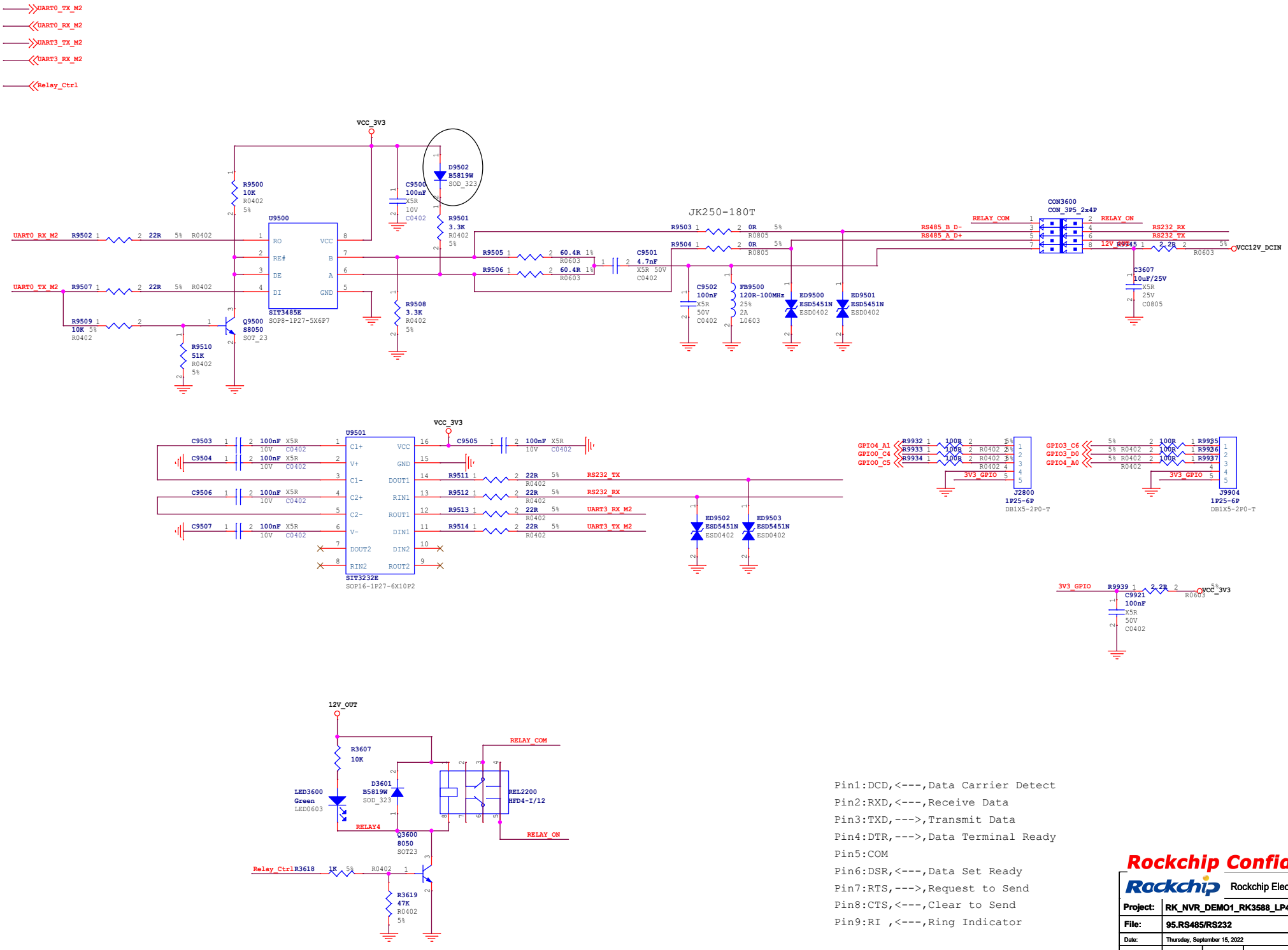
HW_ID



SARADC_VIN1	Up Resistance	Down Resistance	AD value
HW_ID0	10K	DNP	4095
HW_ID1	10K	110K	3754
HW_ID2	20K	100K	3413
HW_ID3	33K	100K	3079
HW_ID4	18K	36K	2730
HW_ID5	36K	51K	2400
HW_ID6	51K	51K	2048
HW_ID7	51K	36K	1695
HW_ID8	36K	18K	1365
HW_ID9	100K	33K	1016
HW_ID10	100K	20K	683
HW_ID11	110K	10K	341
HW_ID12	DNP	10K	0

V10
V21

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	93.HW_ID				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	40 of 43



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	95.RS485/RS232				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	41 of 43

H9900
HOLE_3R20
HOLE_C3R20_C6R00

H9901
HOLE_3R20
HOLE_C3R20_C6R00

H9906
HOLE_3R20
HOLE_C3R20_C6R00

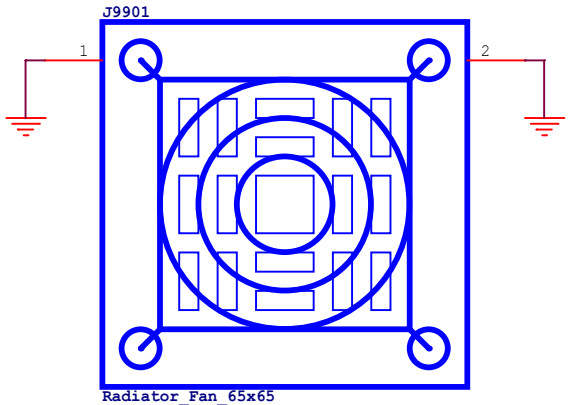
H9909
HOLE_3R20
HOLE_C3R20_C6R00

H9904
HOLE_3R20
HOLE_C3R20_C6R00

H9905
HOLE_3R20
HOLE_C3R20_C6R00

H9907
HOLE_3R20
HOLE_C3R20_C6R00

H9908
HOLE_3R20
HOLE_C3R20_C6R00



Radiator_Fan_65x65
radiator_38rx38rx10rd3

TOP Mark

M9900
MARK
MARK

M9901
MARK
MARK

M9902
MARK
MARK

BOTTOM Mark

M9903
MARK
MARK

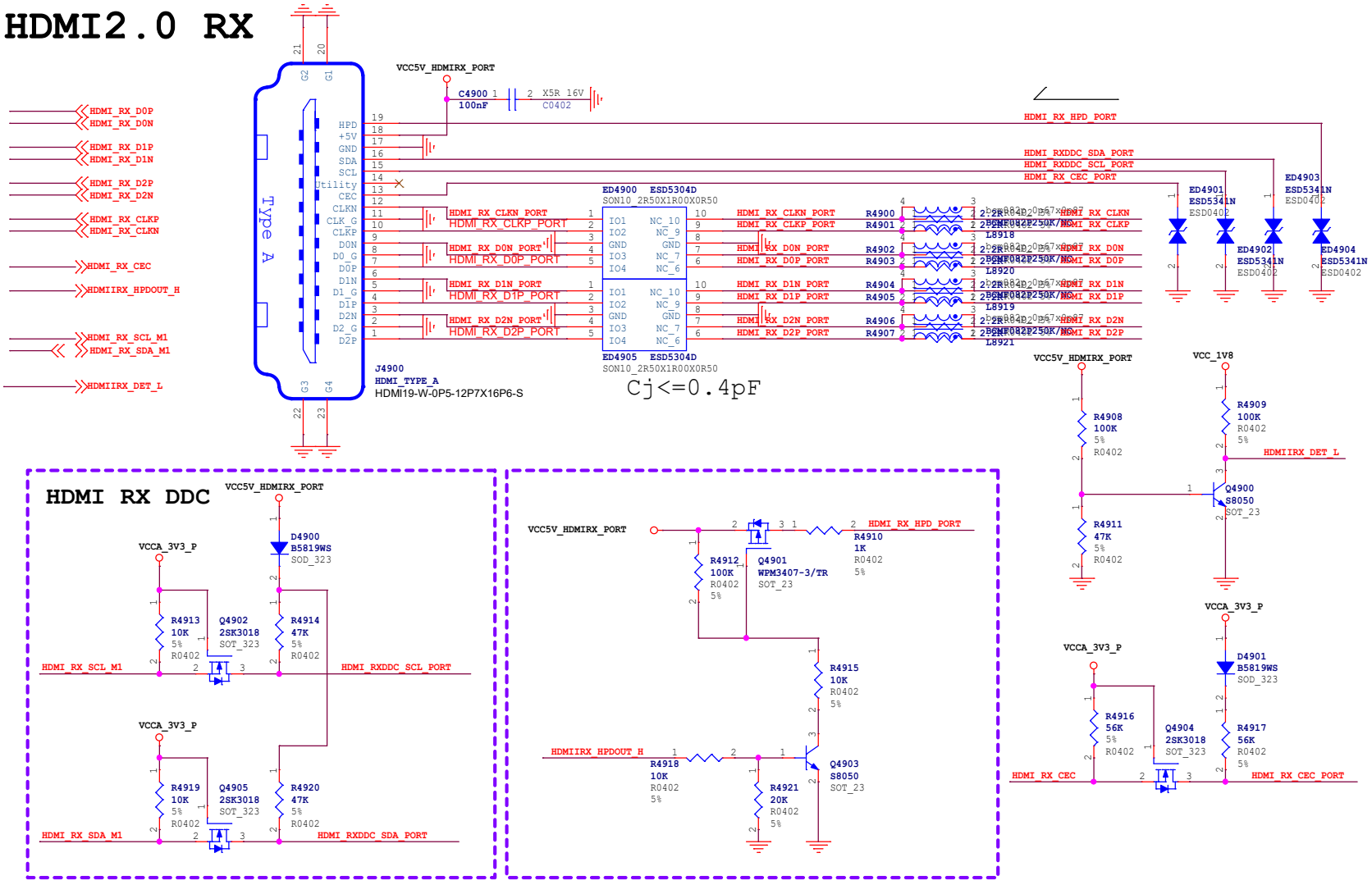
M9904
MARK
MARK

M9905
MARK
MARK

Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21				
File:	99.Mark/Hole/Heatsink				
Date:	Thursday, September 15, 2022			Rev:	V2.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	43 of 43

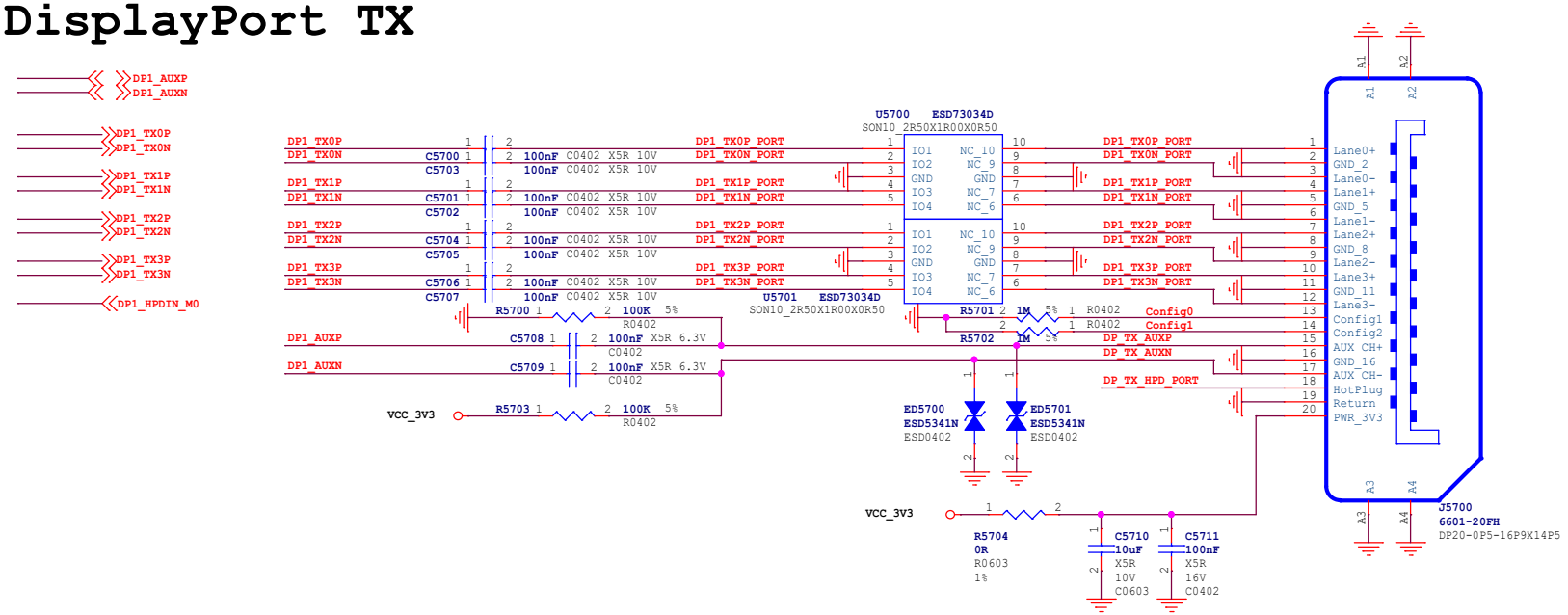
HDMI2.0 RX



HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

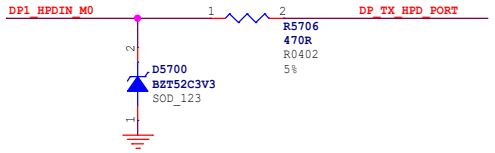
ShenZhen HugSun Technology Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	49.HDMI IN		
Date:	Thursday, September 15, 2022	Rev:	V1.0
Designed by:	Wang	Sheet:	51 of 99

DisplayPort TX



DP_TX_HPD

HPD Voltage:2.25-3.6V



ShenZhen HugSun Technology Co., Ltd			
Project:	RK_NVR_DEMO1_RK3588_LP4/4x_V21		
File:	51.DP		
Date:	Thursday, September 15, 2022	Rev:	V1.0
Designed by:	Wang	Sheet:	51 of 99

WIFI（802.11 a/b/g/n/ac 2x2 MIMO）