Reference Schematics For RK3588S

RK3588S_Tablet_REF_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC or 2Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
4) ROM: eMMC5.1(Default) or SPI Falsh
5) Support: 1 x Micro SD Card3.0
6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
7) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
8) Support: 2 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
10) Support: 2 x 4Lanes MIPI D/CPHY TX
11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
13) Support: 2 x PDM MIC Array
14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

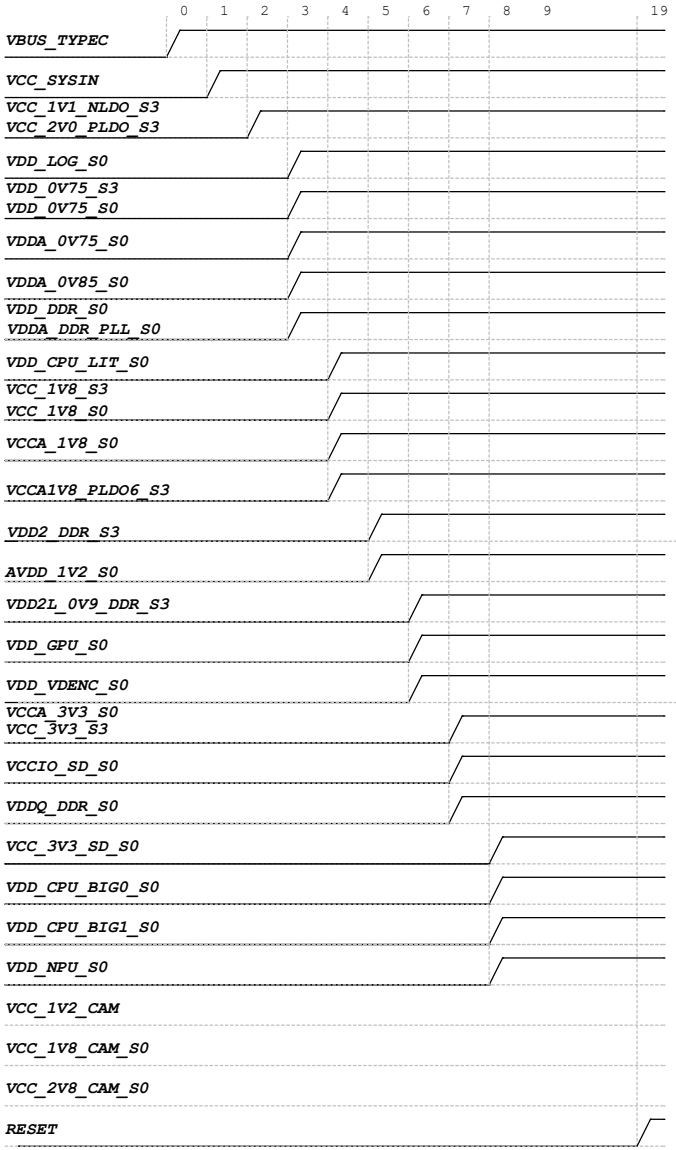
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RP01A				
File:	00.Cover Page				
Date:	Friday, November 14, 2025			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	1 of 40

Revision History

Version	Date	By	Change Dsecription	Approved
V1.01	20251021	WZH	First release REF form EDGE-RK3588S（Blueberry）	
			1:Add ES7210x2 6MIC and 2 AEC	
			2. Delete TF card, Add WiFi for ap6256	
			3. Delete MIPIC CSIx1	
			4. M.2 PCIE E-key change to M-Key	
			5. Add MIPI DSI backlight	

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	02.Revision History		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	2 of 40

Power Sequence

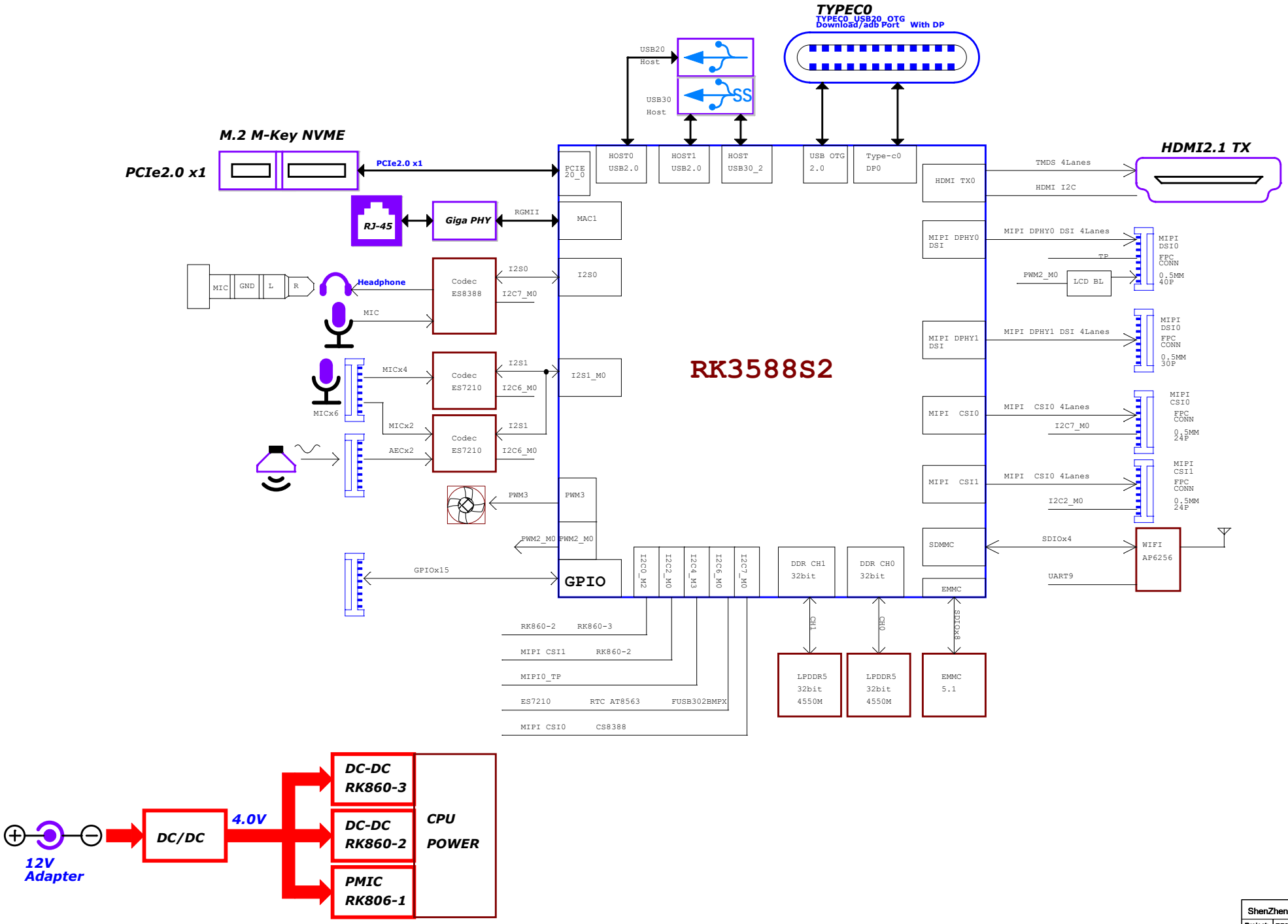


Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2_	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2_	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4_	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5_	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6_	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RP01A				
File:	05.System Power Sequence				
Date:	Friday, November 14, 2025			Rev:	V12
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	5 of 40



ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	04.Block diagram
Date:	Friday, November 14, 2025
Rev:	V1.0
Designed by:	Wang
Sheet:	4 of 40

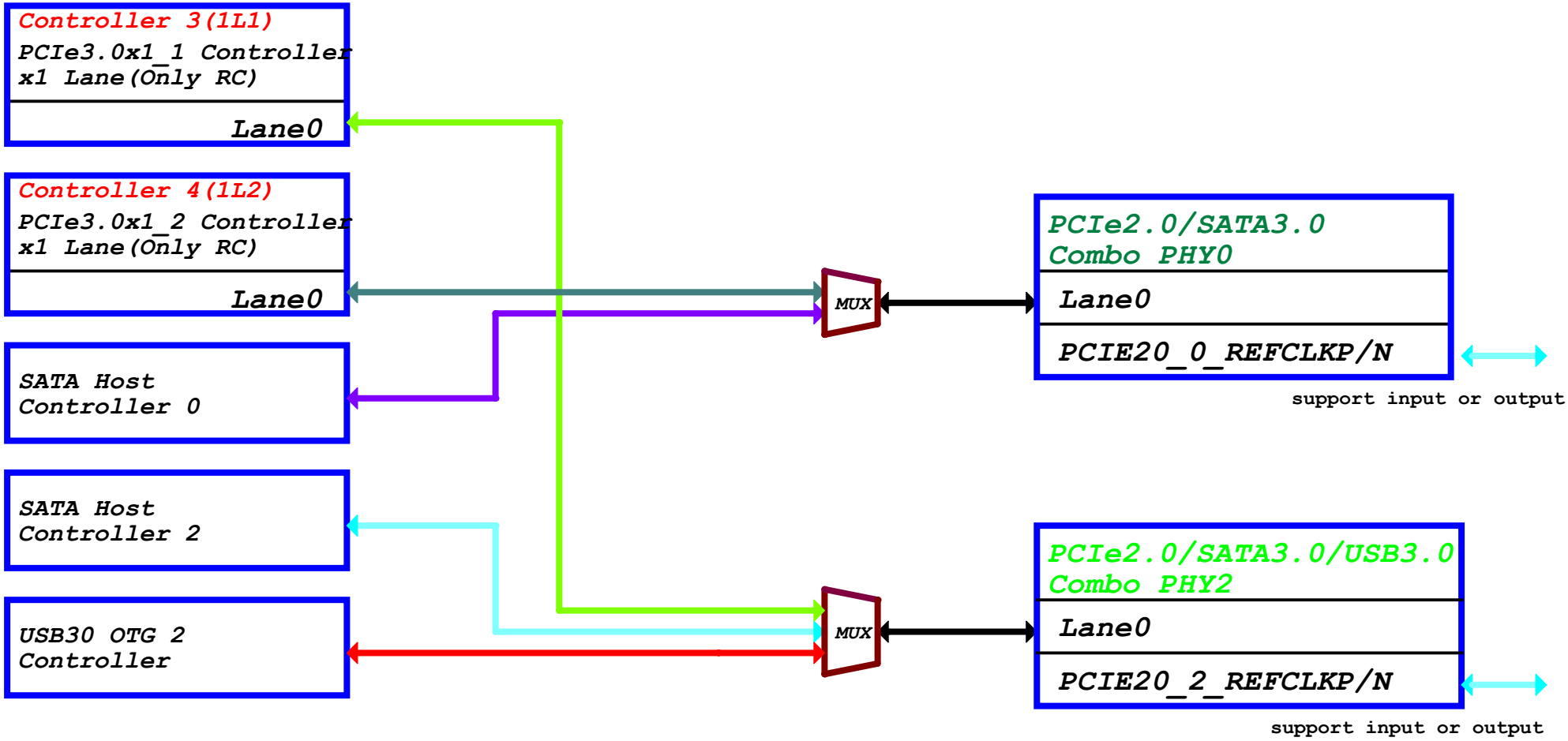
I2C0_M2	RK860-2	RK860-3	
I2C2_M0	MIPI CSI1	RK860-2	
I2C3_M0	GPIO_预留		
I2C4_M3	MIPI0_TP		
I2C5_M3	GPIO_预留		
I2C6_M0	ES7210	RTC AT8563	FUSB302BMPX
I2C7_M0	MIPI CSI0	CS8388	

UART0_M2	GPIO_预留
UART2_M0	Debug
UART3_M0	GPIO_预留
UART7_M2	GPIO_预留
UART9_M2	BT

PWM2_M0	LCD BL
PWM11_M2	GPIO_预留
PWM12_M1	GPIO_预留
PWM13_M2	GPIO_预留
PWM14_M1	GPIO_预留
PWM15_M2	GPIO_预留

ShenZhen HugSun Technology Co., Ltd			
Project:	**RP01A**		
File:	**06.I2C Map/Uart Map**		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	6 of 40

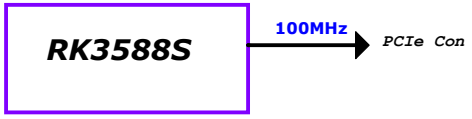
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



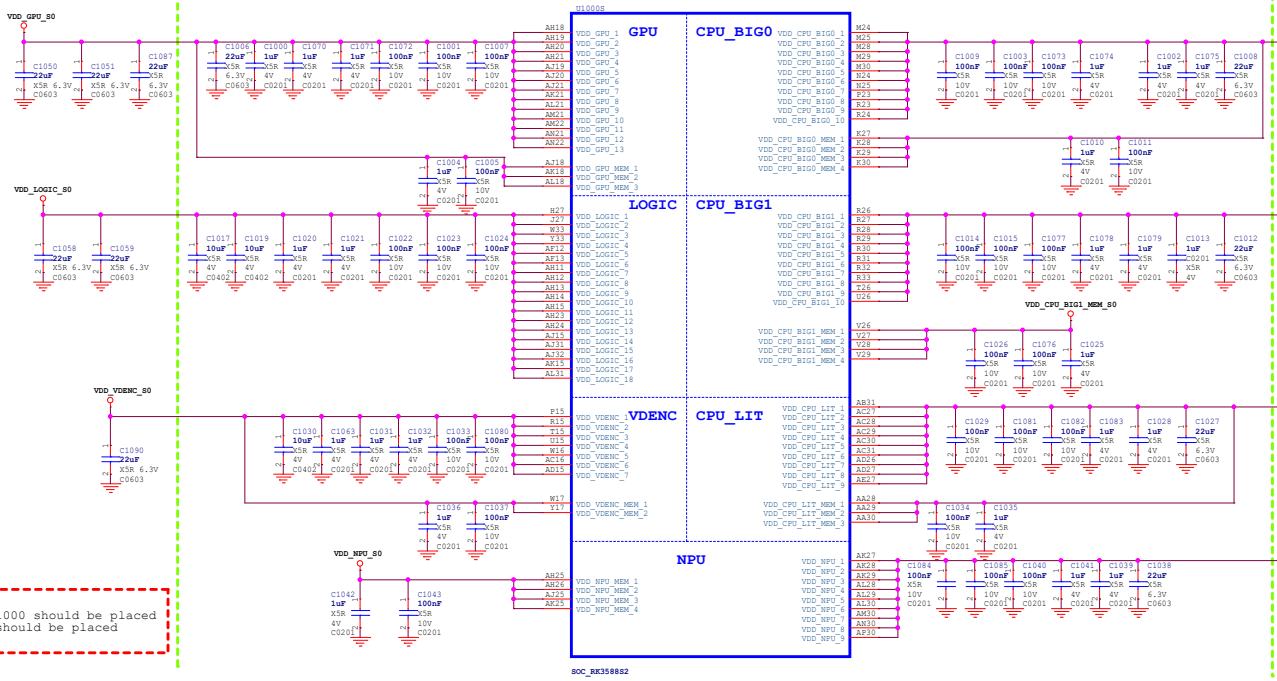
Note:

PCIE20_*_REFCLKP/N is output or input gpio

M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

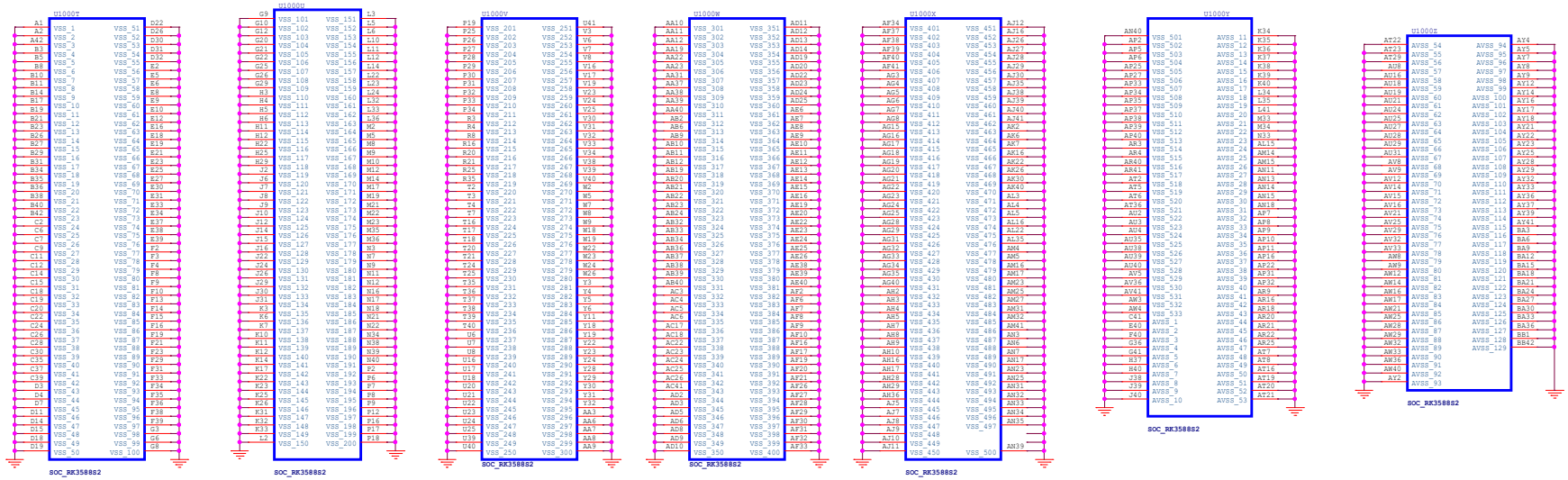
ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	08.PCIE Fun Map		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	8 of 40

RK3588S(Power&Gnd)



Note:

The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	10.RK3588S_Power/GND
Date:	Friday, November 14, 2025
Rev:	V1.0
Designed by:	Wang
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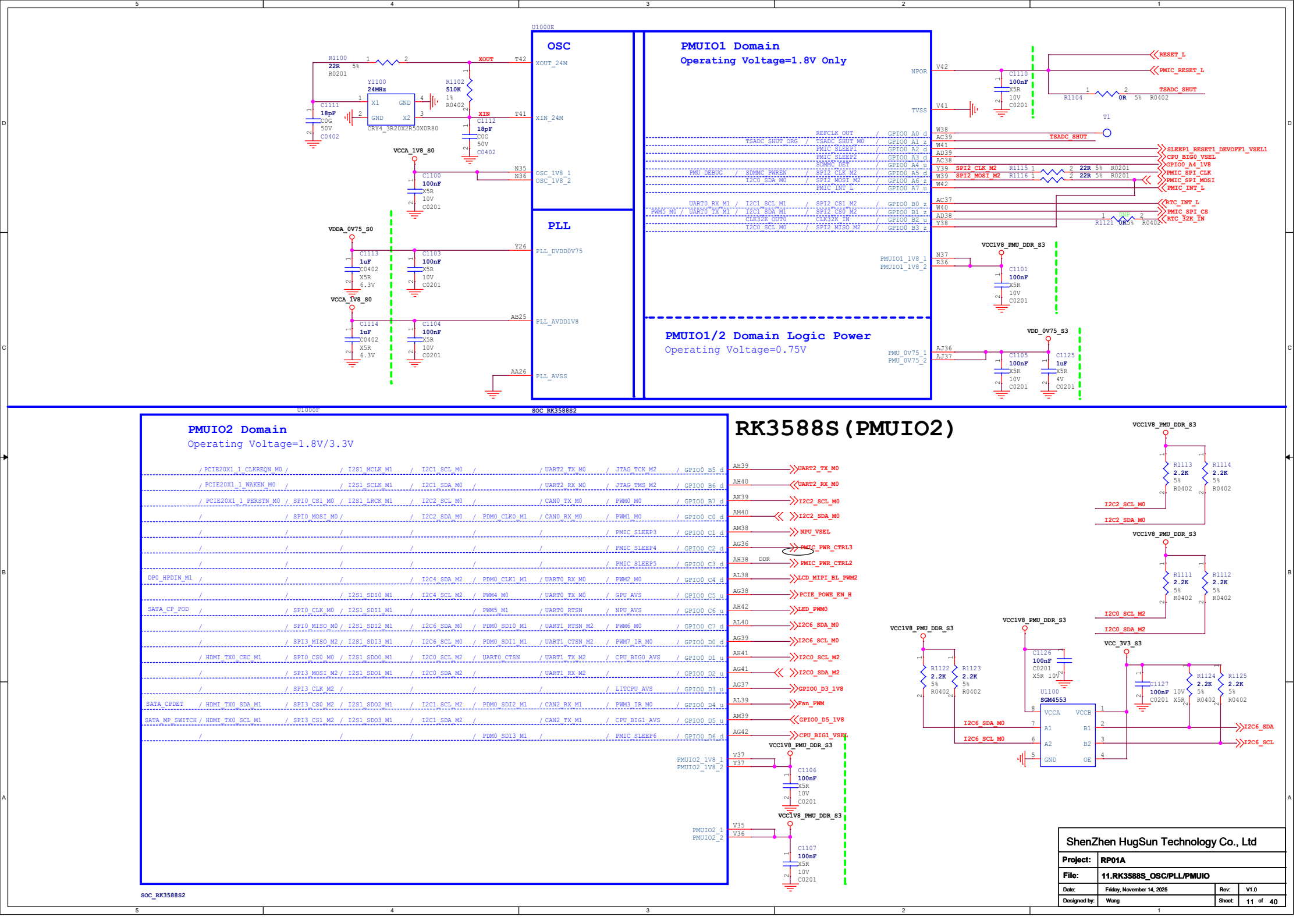
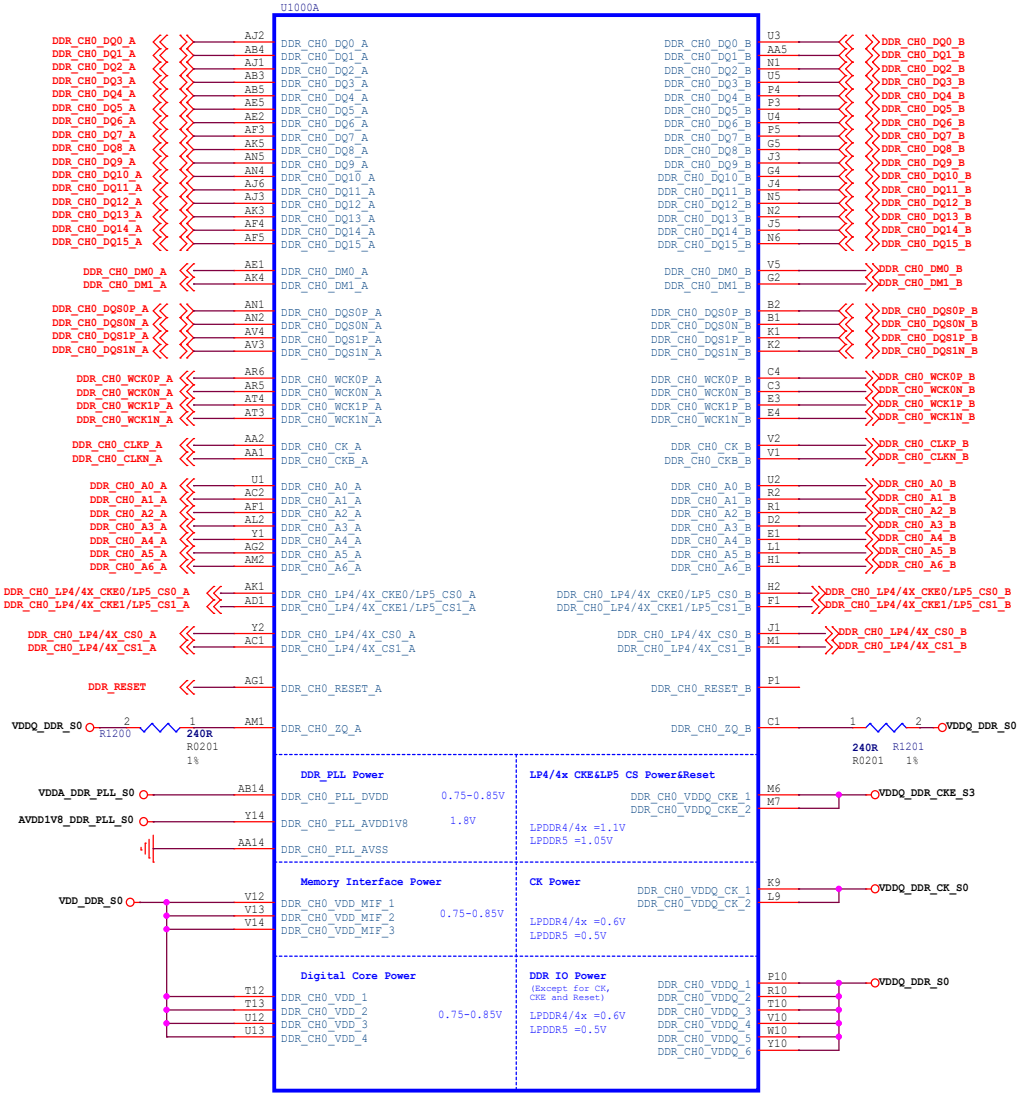
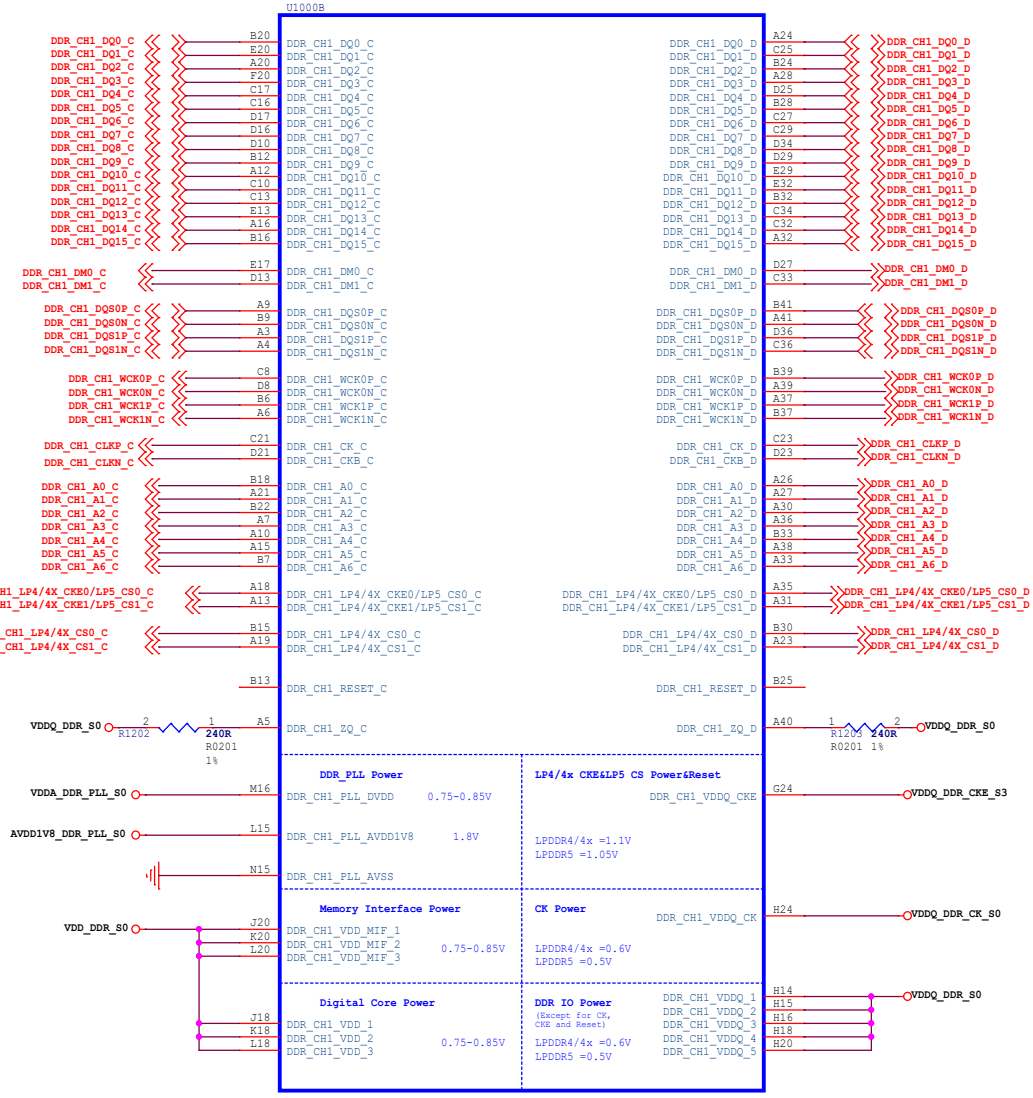
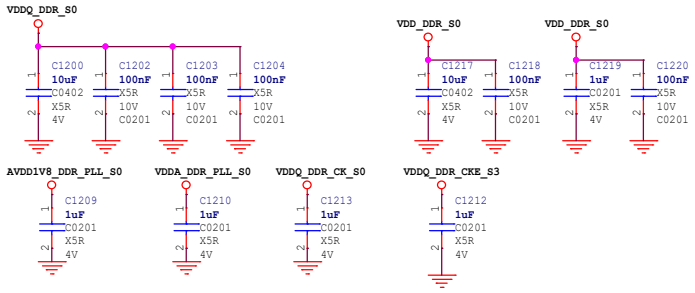

U1000E
OSC
XOUT_24M
XIN_24M
PLL
PLL_DVDD0V75
PLL_AVDD1V8
PLL_AVSS
OSC_1V8_1
OSC_1V8_2
PMUIO1 Domain
Operating Voltage=1.8V Only
PMUIO1/2 Domain Logic Power
Operating Voltage=0.75V
U1000F
SOC_RK3588S2
PMUIO2 Domain
Operating Voltage=1.8V/3.3V
RK3588S(PMUIO2)
ShenZhen HugSun Technology Co., Ltd
Project: RP01A
File: 11.RK3588S_OSC/PLL/PMUIO
Date: Friday, November 14, 2025
Rev: V1.0
Designed by: Wang
Sheet: 11 of 40

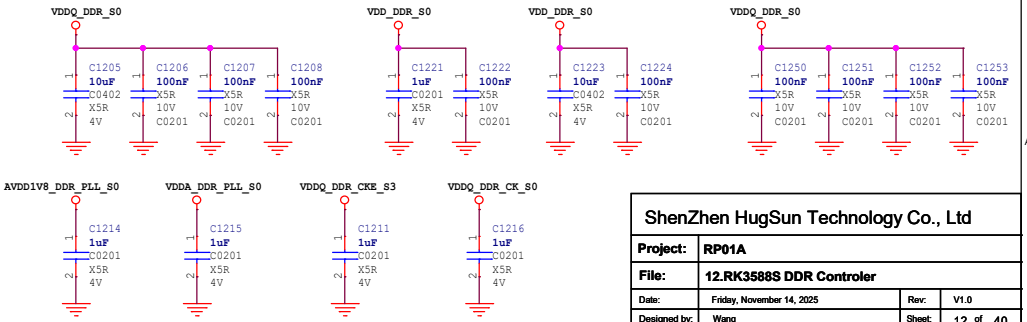
RK3588S(DDR PHY)





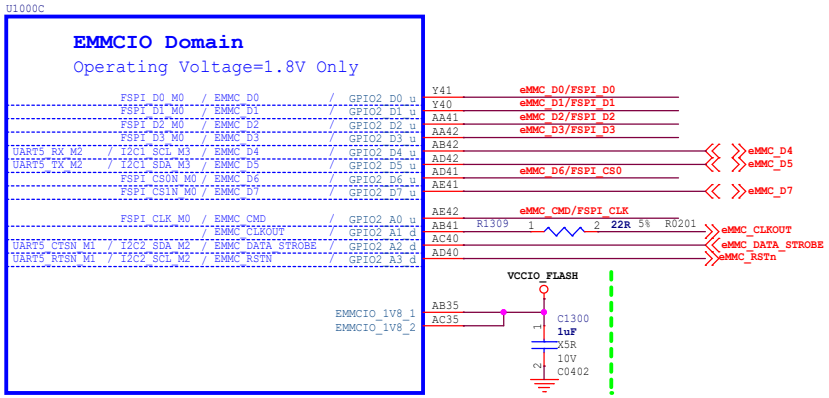
DDR FILTER





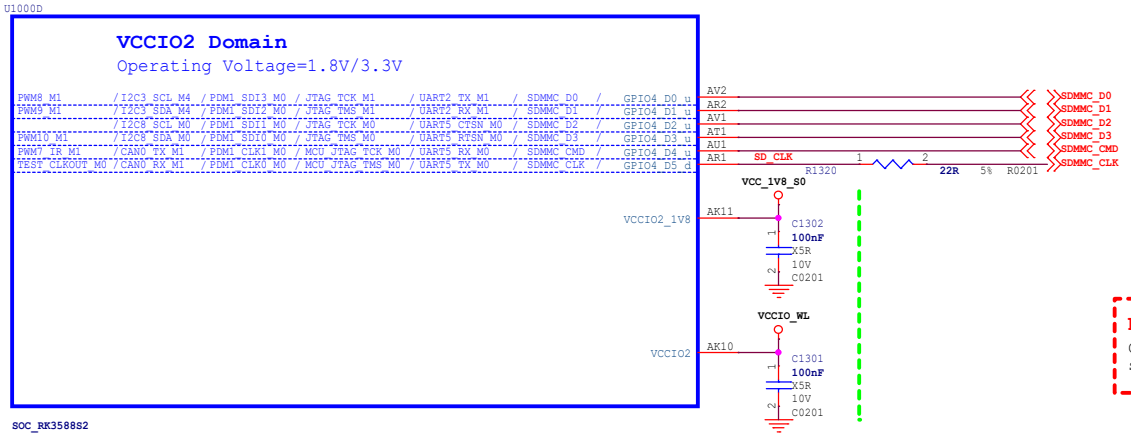
ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	12.RK3588S DDR Controler		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	12 of 40

RK3588S(EMMCIO Domain)



Default:eMMC

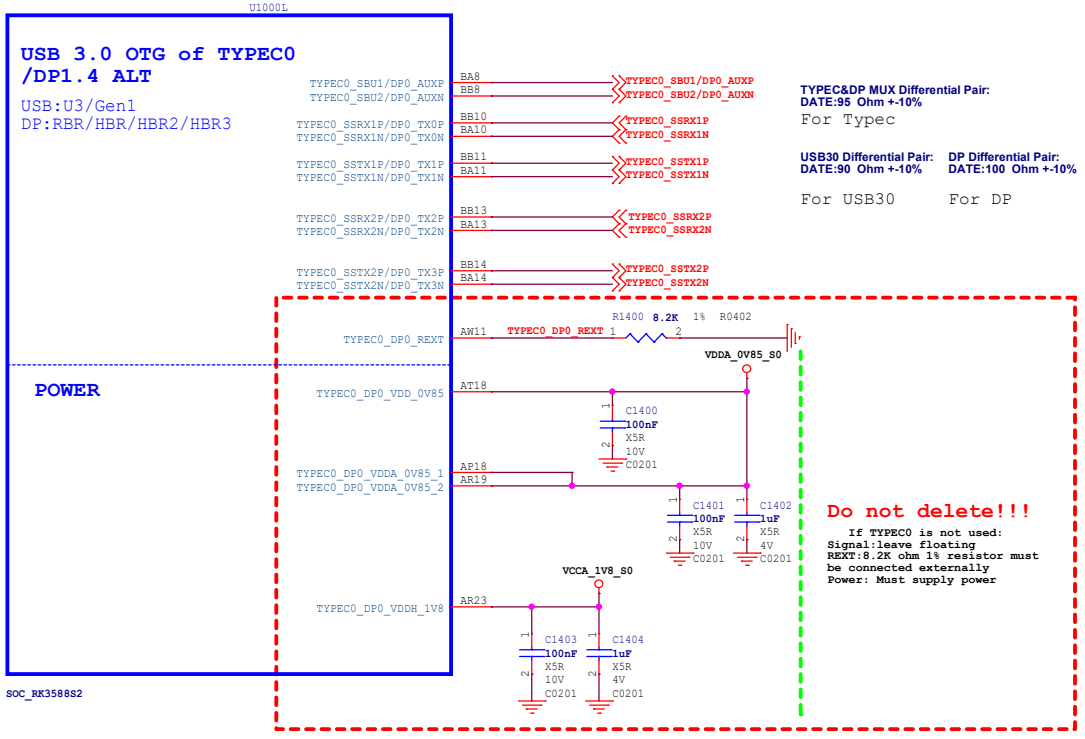
RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	13.RK3588S Flash/SD Controller		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	13 of 40

RK3588S(USB3.0/DP1.4)

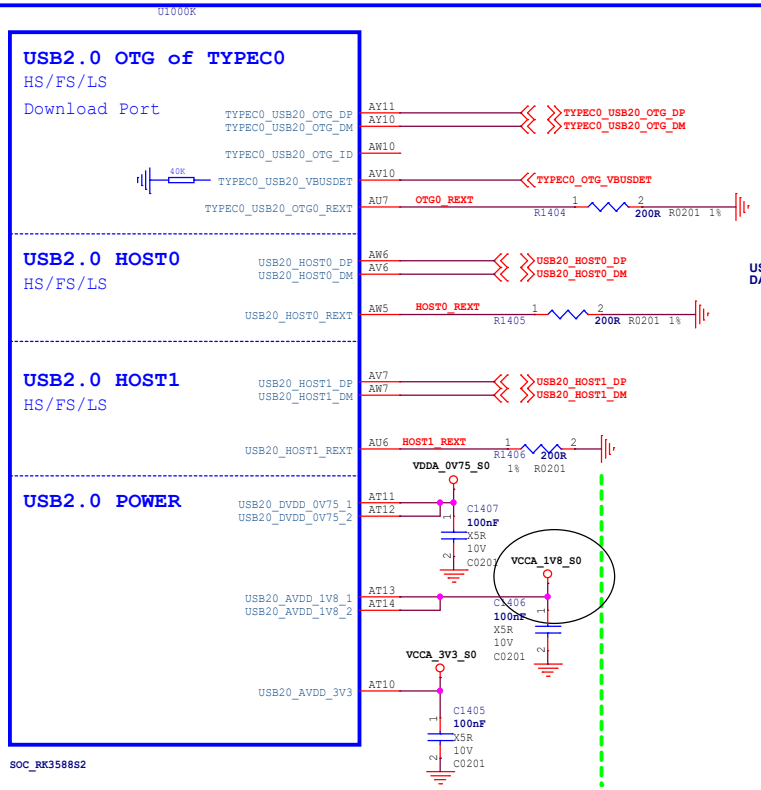


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

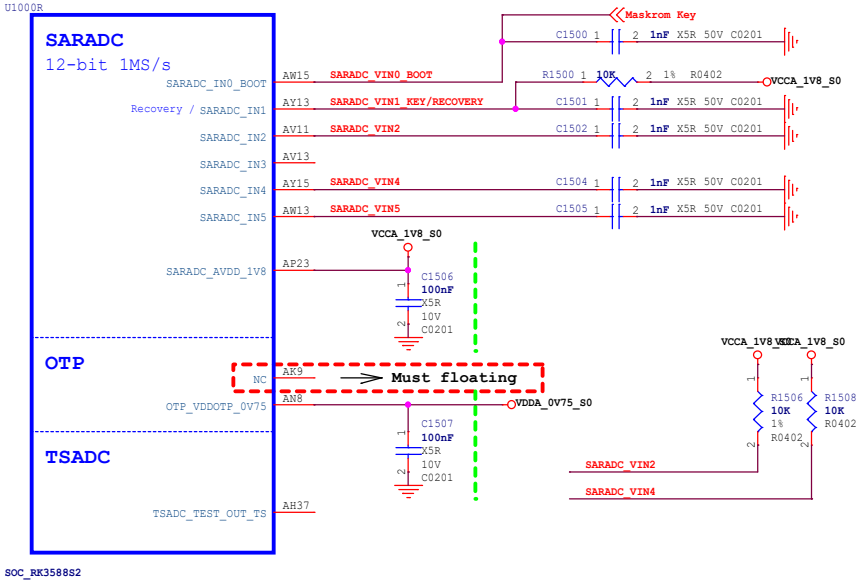
USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating

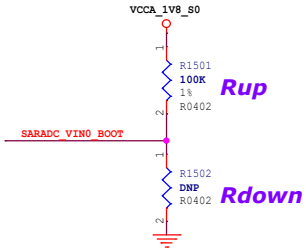
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	14.RK3588S_USB20/USB30/DP PHY		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	14 of 40

RK3588S(SARADC/OTP/TSADC)

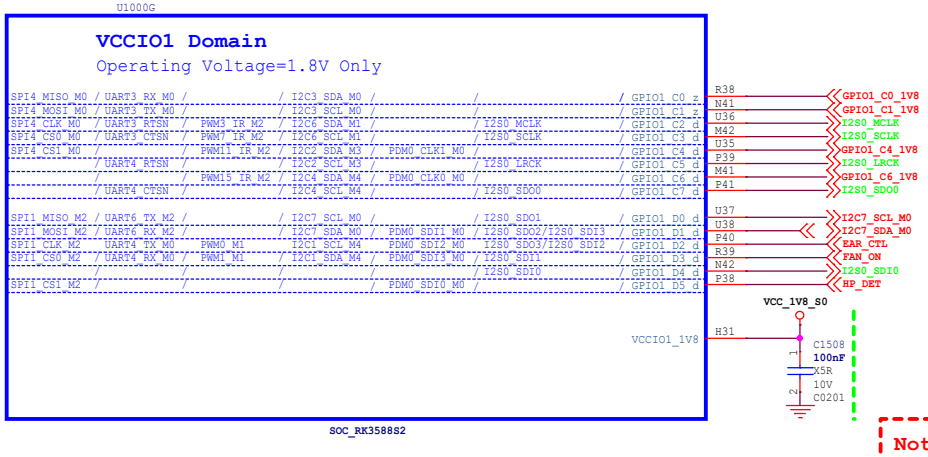


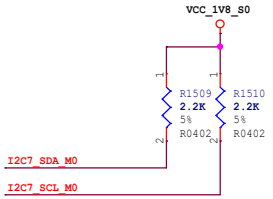
BOOT MODE CONFIG



Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

RK3588S(VCCIO1 Domain)

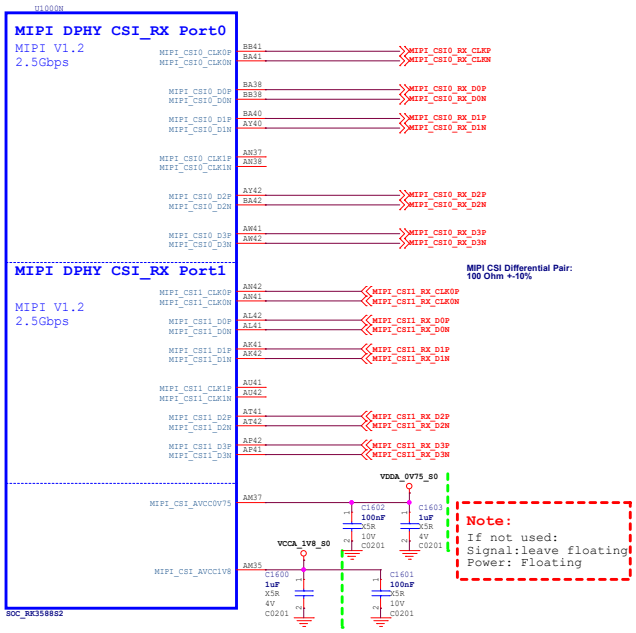




Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	15.RK3588S_SARADC/1.8V GPIO		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	15 of 40

RK3588S(MIPI_DPHY CSI0 RX)

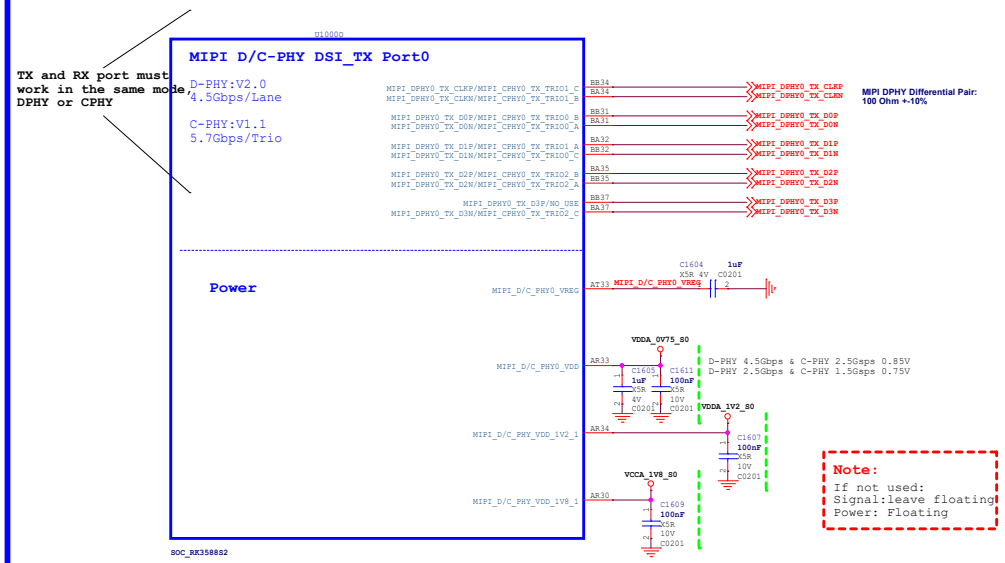


Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

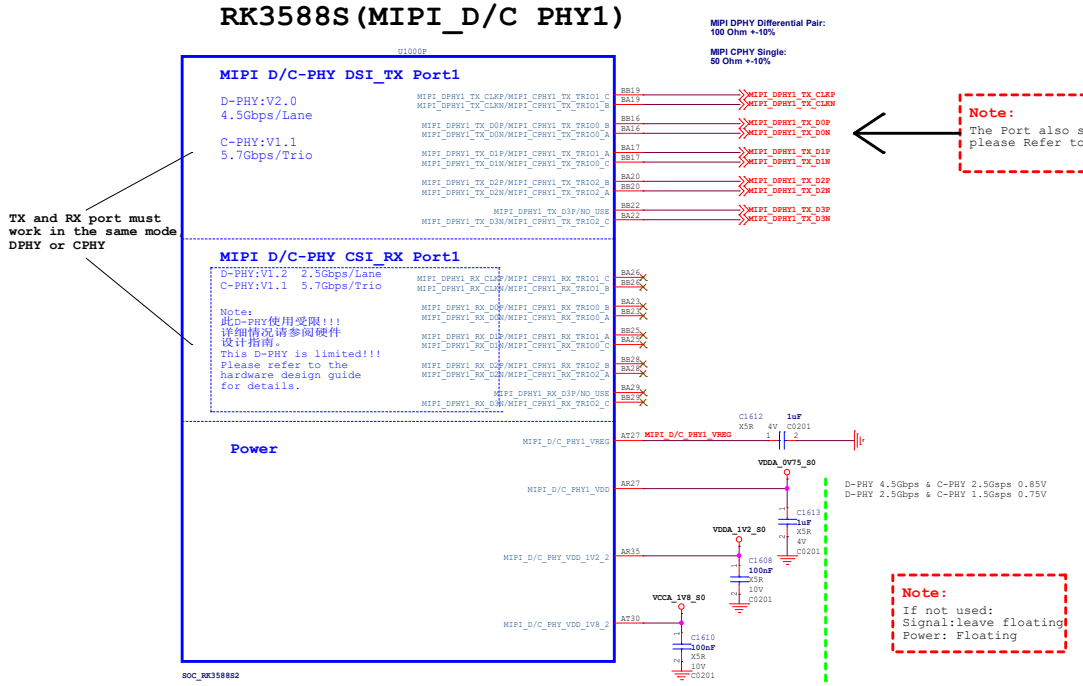
Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)



RK3588S(MIPI_D/C PHY1)



ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	16.RK3588S_MIPI Interface
Date: Friday, November 14, 2025	Rev: V1.0
Designed by: Wang	Sheet 16 of 40

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

U1000Q

HDMI TX/eDP1.3 MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_D0P/EDP_TX0_D0P	BB4	EDP_TX0_D0P/HDMI0_TX0P
HDMI_TX0_D0N/EDP_TX0_D0N	BA4	EDP_TX0_D0N/HDMI0_TX0N
HDMI_TX0_D1P/EDP_TX0_D1P	BA5	EDP_TX0_D1P/HDMI0_TX1P
HDMI_TX0_D1N/EDP_TX0_D1N	BB5	EDP_TX0_D1N/HDMI0_TX1N
HDMI_TX0_D2P/EDP_TX0_D2P	BB7	EDP_TX0_D2P/HDMI0_TX2P
HDMI_TX0_D2N/EDP_TX0_D2N	BA7	EDP_TX0_D2N/HDMI0_TX2N
HDMI_TX0_D3P/EDP_TX0_D3P	BA2	EDP_TX0_D3P/HDMI0_TX3P
HDMI_TX0_D3N/EDP_TX0_D3N	BB2	EDP_TX0_D3N/HDMI0_TX3N
HDMI_TX0_SBDP/EDP_TX0_AUXP	BA1	EDP_TX0_AUXP/HDMI0_TX_SBDP
HDMI_TX0_SBDN/EDP_TX0_AUXN	AY1	EDP_TX0_AUXN/HDMI0_TX_SBDN

POWER

HDMI/eDP_TX0_REXT — AY3 HDMI/eDP_TX0_REXT — R1708 1 — 2 8.2K 1% R0402 — HDMI_VDDA0V85_S0

HDMI/EDP_TX0_VDD_0V75_1 AM13
HDMI/EDP_TX0_VDD_0V75_2 AN12
C1710 100nF X5R 10V C0201
C1711 4.7uF X5R 6.3V C0402
C1718 Actual Setting 0.8375V 10uF X5R 6.3V C0603

HDMI/EDP_TX0_AVDD_0V75 AN10
C1712 100nF X5R 10V C0201
C1725 1uF X5R 4V C0201

VCCA_1V8_S0

HDMI/EDP_TX0_VDD_IO_1V8 AK12
HDMI/EDP_TX0_VDD_CMN_1V8 AL14
C1713 100nF X5R 10V C0201
C1714 4.7uF X5R 6.3V C0402
C1716 4.7uF X5R 6.3V C0402

SOC_RK3588S2

HDMI TX
100 Ohm ±10%

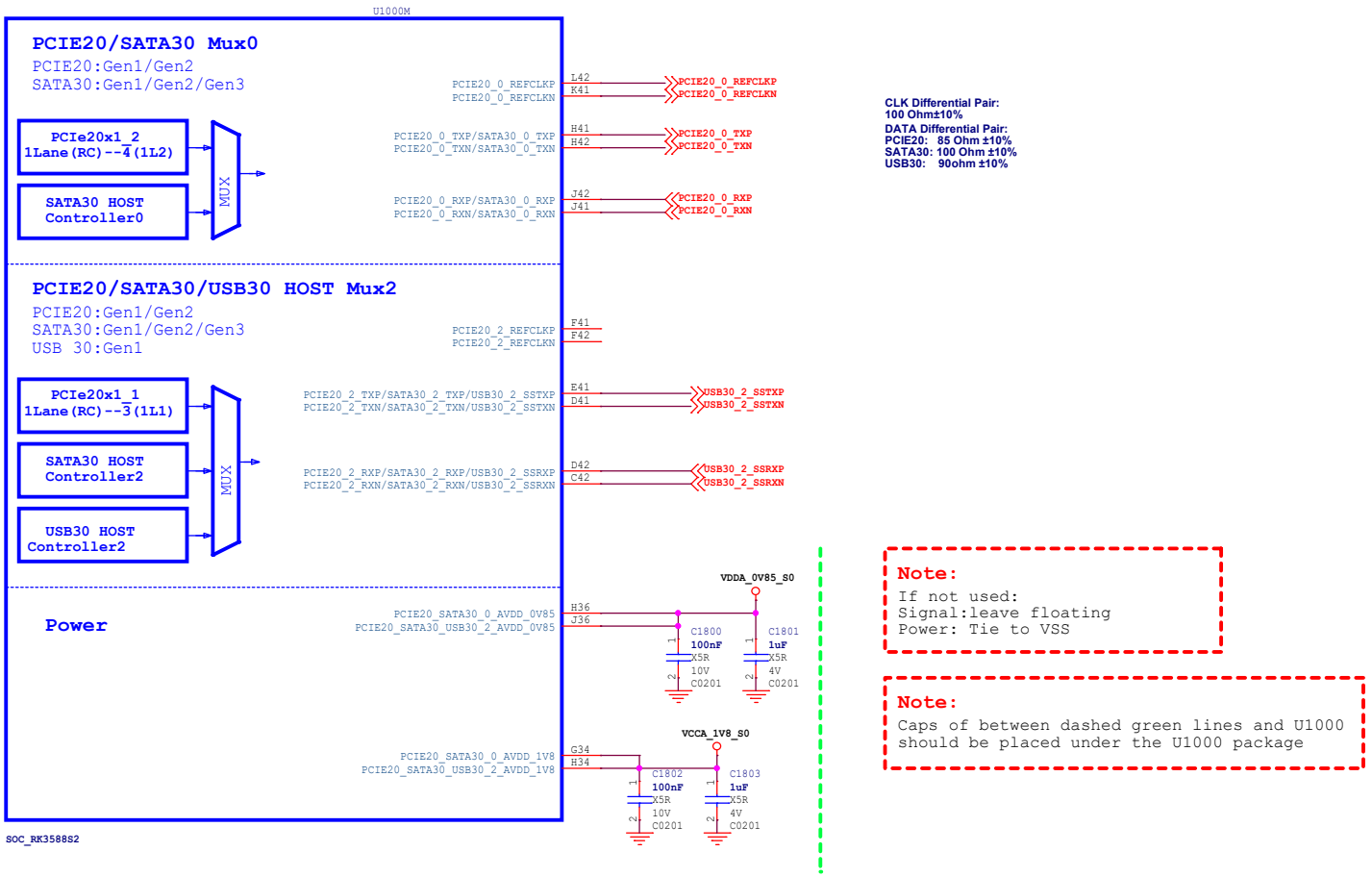
EDP_TX0_D0P/HDMI0_TX0P	HDMI0_TX0P
EDP_TX0_D0N/HDMI0_TX0N	HDMI0_TX0N
EDP_TX0_D1P/HDMI0_TX1P	HDMI0_TX1P
EDP_TX0_D1N/HDMI0_TX1N	HDMI0_TX1N
EDP_TX0_D2P/HDMI0_TX2P	HDMI0_TX2P
EDP_TX0_D2N/HDMI0_TX2N	HDMI0_TX2N
EDP_TX0_D3P/HDMI0_TX3P	HDMI0_TX3P
EDP_TX0_D3N/HDMI0_TX3N	HDMI0_TX3N
EDP_TX0_AUXP/HDMI0_TX_SBDP	HDMI0_TX_SBDP
EDP_TX0_AUXN/HDMI0_TX_SBDN	HDMI0_TX_SBDN

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	17.RK3588S_HDMI/eDP Interface		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	17 of 40

RK3588S(PCIE20/SATA30/USB30)



Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	18.RK3588S PCIE2/SATA3/USB3 PHY		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	18 of 40

RK3588S(VCCIO4 Domain)

U1000H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

PCIE20X1_1_CLKREQN_M2	SPDIF0_TX_M0	UART6_RX_M1	SPI4_MISO_M2	I2C2_SDA_M4	GPIO1_A0_d	G40	LCD_MIPI_PW_EN1
PCIE20X1_1_WAKEN_M2		UART6_TX_M1	SPI4_MOSI_M2	I2C2_SCL_M4	GPIO1_A1_d	L40	TP_RST1
PWM0_M2	VOP_POST_EMPTY	UART6_RTSN_M1	SPI4_CLK_M2	I2C4_SDA_M3	GPIO1_A2_d	D38	I2C4_SDA_M3
PWM1_M2		UART6_CTSN_M1	SPI4_CS0_M2	I2C4_SCL_M3	GPIO1_A3_d	L39	I2C4_SCL_M3
			SPI2_MISO_M0		GPIO1_A4_d	G37	T4
	HDMI_TX0_HPD_M0		SPI2_MOSI_M0		GPIO1_A5_d	M40	HDMI_TX0_HPD_M0
			SPI2_CLK_M0		GPIO1_A6_d	D39	MIPI_CAM2_RST_L
PWM3_IR_M3 / PCIE20X1_1_PERSTN_M2			SPI2_CS0_M0 / PDM1_SDI0_M1		GPIO1_A7_u	H38	TP_INT1
			SPI2_CS1_M0 / PDM1_SDI1_M1		GPIO1_B0_u	H39	LCD_MIPI_TE2
			SPI0_MISO_M2 / PDM1_SDI2_M1		GPIO1_B1_d	G39	LCD_MIPI_RESET1
		UART4_RX_M2	SPI0_MOSI_M2 / PDM1_SDI3_M1		GPIO1_B2_d	M38	MIPI_CAM1_RST_L
	SATA0_ACT_LED_M1	UART4_TX_M2	SPI0_CLK_M2 / PDM1_CLK1_M1		GPIO1_B3_d	M37	LCD_MIPI_RESET2
		UART7_RX_M2	SPI0_CS0_M2 / PDM1_CLK0_M1		GPIO1_B4_u	M39	GPIO1_B4_1V8
		UART7_TX_M2	SPI0_CS1_M2 /		GPIO1_B5_u	D40	GPIO1_B5_1V8
	MIPI_CAMERA1_CLK_M0	UART1_TX_M1	SPDIF0_TX_M0 / I2C5_SCL_M3		GPIO1_B6_u	L38	GPIO1_B6_1V8
PWM13_M2	SATA2_ACT_LED_M1	MIPI_CAMERA2_CLK_M0	UART1_RX_M1	SPDIF1_TX_M0 / I2C5_SDA_M3	GPIO1_B7_u	F37	GPIO1_B7_1V8
PWM14_M2		MIPI_CAMERA3_CLK_M0	UART1_RTSN_M1	I2C8_SCL_M2	GPIO1_D6_u	L37	MIPI_CAM3_CLKOUT
PWM15_IR_M3		MIPI_CAMERA4_CLK_M0	UART1_CTSN_M1	I2C8_SDA_M2	GPIO1_D7_u	G38	MIPI_CAM4_CLKOUT

VCC_1V8_S0

VCCIO4_1V8_1 G27
VCCIO4_1V8_2 G28
C1902 100nF X5R 10V C0201

VCC_1V8_S0

VCCIO4 G31
C1903 100nF X5R 10V C0201

SOC_RK3588S

VCC_1V8_S0

R10000 2.2K 5% R0402
R10001 2.2K 5% R0402

I2C4_SDA_M3
I2C4_SCL_M3

RK3588S(VCCIO6 Domain)

U1000J

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

BT1120_D0	CIF_D0		I2S1_MCLK_M0	UART9_RTSN_M1	SPI0_MISO_M1	PCIE20X1_1_CLKREQN_M1	GPIO4_A0_d	AV19	I2S1_MCLK
BT1120_D1	CIF_D1		I2S1_SCLK_M0	UART9_CTSN_M1	SPI0_MOSI_M1	PCIE20X1_1_WAKEN_M1	GPIO4_A1_d	AW18	I2S1_SCLK_TX
BT1120_D2	CIF_D2		I2S1_LRCK_M0		SPI0_CLK_M1	PCIE20X1_1_PERSTN_M1	GPIO4_A2_d	AV26	I2S1_LRCK_TX
BT1120_D3	CIF_D3			UART0_TX_M2			GPIO4_A3_d	AV19	GPIO4_A3_3V3
BT1120_D4	CIF_D4			UART0_RX_M2	SPI2_MISO_M1 / I2C3_SCL_M2		GPIO4_A4_d	AW19	GPIO4_A4_3V3
BT1120_D5	CIF_D5		I2S1_SDI0_M0	UART3_TX_M2	SPI2_MOSI_M1 / I2C3_SDA_M2		GPIO4_A5_d	AU15	I2S1_SDI0
BT1120_D6	CIF_D6		I2S1_SDI1_M0	UART3_RX_M2	SPI2_CLK_M1 / I2C5_SCL_M2		GPIO4_A6_d	AV18	I2S1_SDI1
BT1120_D7	CIF_D7		I2S1_SDI2_M0		SPI2_CS0_M1 / I2C5_SDA_M2		GPIO4_A7_d	AW26	I2S1_SDI2
BT1120_CLKOUT	CIF_CLKIN		I2S1_SDI3_M0	UART9_TX_M0	SPI2_CS1_M1 / I2C6_SDA_M3		GPIO4_B0_d	AW27	I2S1_SDI3
SPDIF1_TX_M1	MIPI_CAMERA0_CLK_M0 / SATA2_ACT_LED_M0		I2S1_SDO0_M0	UART9_RX_M0	SPI0_CS1_M1 / I2C6_SCL_M3		GPIO4_B1_u	AU22	TYPEC0_SBU1_DC
CAN1_RX_M1	BT1120_D8	CIF_HREF	PWM14_M1	I2S1_SDO1_M0	UART8_RTSN_M0	SPI0_CS0_M1 / I2C7_SCL_M3	PCIE20X1_1_BUTTON_RSTN / GPIO4_B2_u	AT15	GPIO4_B2_3V3
CAN1_TX_M1	BT1120_D9	CIF_VSYNC	PWM15_IR_M1	I2S1_SDO2_M0	UART8_CTSN_M0	I2C7_SDA_M3	PCIE20X1_2_BUTTON_RSTN / GPIO4_B3_u	AW23	SBBC_INT_L
BT1120_D10	CIF_CLKOUT		PWM11_IR_M1	I2S1_SDO3_M0	UART9_TX_M1	DP0_HPDIN_M0 / SPDIF0_TX_M1	GPIO4_B4_u	AV27	TYPEC0_SBU2_DC
BT1120_D11			PWM12_M1		UART9_RX_M1	SPI3_MISO_M1	GPIO4_B5_d	AW23	GPIO4_B5_3V3
BT1120_D12			PWM13_M1			SPI3_MOSI_M1 / I2C5_SCL_M1 / SATA0_ACT_LED_M0	GPIO4_B6_d	AW22	HDMI0_TX_ON_H
BT1120_D13			HDMI_TX0_SCL_M0			SPI3_CLK_M1 / I2C5_SDA_M1 / PCIE20X1_2_CLKREQN_M1	GPIO4_B7_u	AV22	HDMI_TX0_SCL_M0
BT1120_D14			HDMI_TX0_SDA_M0			SPI3_CS0_M1 / I2C8_SCL_M3 / PCIE20X1_2_WAKEN_M1	GPIO4_C0_u	AW23	HDMI_TX0_SDA_M0
BT1120_D15	SPDIF1_TX_M2	PWM6_M1	HDMI_TX0_CEC_M0		SPI3_CS1_M1 / I2C8_SDA_M3 / PCIE20X1_2_PERSTN_M1		GPIO4_C1_d	AW26	HDMI_TX0_CEC_M0

Note:
BT1120 Only Support Output

VCC_1V8_S0

VCCIO6_1V8 AJ34
C1906 100nF X5R 10V C0201

VCC_3V3_S0

VCCIO6_1 AL33
VCCIO6_2 AM33
C1907 100nF X5R 10V C0201

SOC_RK3588S

RK3588S(VCCIO5 Domain)

U1000I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1 / I2C6_SDA_M4	GMAC1_TXD2	I2S3_MCLK	FSPI_D0_M2	SDIO_D0_M1	GPIO3_A0_u	AR38	GMAC0_TXD2
AUDDSM_LN / PWM11_IR_M0	SPI4_MOSI_M1 / I2C6_SCL_M4	GMAC1_TXD3	I2S3_SCLK	FSPI_D1_M2	SDIO_D1_M1	GPIO3_A1_u	AR37	GMAC0_TXD3
AUDDSM_LP / UART8_TX_M1	SPI4_CLK_M1 /	GMAC1_RXD2	I2S3_LRCK	FSPI_D2_M2	SDIO_D2_M1	GPIO3_A2_u	AT38	GMAC0_RXD2
AUDDSM_RN / UART8_RX_M1	SPI4_CS0_M1 /	GMAC1_RXD3	I2S3_SDO	FSPI_D3_M2	SDIO_D3_M1	GPIO3_A3_u	AT40	GMAC0_RXD3
AUDDSM_RP / UART8_RTSN_M1	SPI4_CS1_M1 /	GMAC1_TXCLK	I2S3_SDI		SDIO_CMD_M1	GPIO3_A4_d	AT39	GMAC0_TXCLK
UART8_CTSN_M1 /	I2C4_SDA_M0 /	GMAC1_RXCLK		FSPI_CLK_M2	MIPI_CAMERA0_CLK_M1 / SDIO_CLK_M1	GPIO3_A5_d	AV38	GMAC0_RXCLK
/	I2C4_SCL_M0 /	ETH1_REFCLKO_25M			MIPI_CAMERA1_CLK_M1 /	GPIO3_A6_d	AV37	BT_REG_ON_H
/	/	GMAC1_RXD0	/		MIPI_CAMERA2_CLK_M1 / PWM8_M0	GPIO3_A7_u	AT37	GMAC0_RXD0
/	/	GMAC1_RXD1	/		MIPI_CAMERA3_CLK_M1 / PWM9_M0	GPIO3_B0_u	AR39	GMAC0_RXD1
UART2_TX_M2	/	GMAC1_RXDV_CRS	/		MIPI_CAMERA4_CLK_M1 / PWM2_M1	GPIO3_B1_d	AV39	GMAC0_RXDV_CRS
UART2_RX_M2	/	GMAC1_TXER	I2S2_SDI_M1	/	PWM3_IR_M1	GPIO3_B2_d	AM34	GMAC0_RSTn_L
UART3_RTSN	/	GMAC1_TXD0	I2S2_SDO_M1	/	/	GPIO3_B3_u	AM35	GMAC0_TXD0
UART3_CTSN	/	GMAC1_TXD1	I2S2_MCLK_M1	/	/	GPIO3_B4_u	AV35	GMAC0_TXD1
UART3_TX_M1	/ CAN1_RX_M0 /	GMAC1_TXEN	I2S2_SCLK_M1	/	PWM12_M0	GPIO3_B5_u	AV35	GMAC0_TXEN
UART3_RX_M1	/ CAN1_TX_M0 /	GMAC1_MCLKINOUT	I2S2_LRCK_M1	/	PWM13_M0	GPIO3_B6_d	AM37	GMAC0_MCLKINOUT
/	SPI1_MOSI_M1 / I2C3_SCL_M1 /	GMAC1_PTP_REF_CLK	/	/	/	GPIO3_B7_d	AY34	WIFI_REG_ON_H
UART7_TX_M1	SPI1_MISO_M1 / I2C3_SDA_M1 /	GMAC1_PPSTRIG	/	/	/	GPIO3_C0_d	AR36	USB_OTG_PWREN
UART7_RX_M1	/ SPI1_CLK_M1 /	GMAC1_PPSCLK	/	/	/	GPIO3_C1_d	AM38	MIPI_CAM1_PDN_L
UART7_RTSN_M1 / SPI1_CS0_M1 /	I2C8_SCL_M4 /	GMAC1_MDC	/	MIPI_TE0	PWM14_M0	GPIO3_C2_d	AV40	GMAC0_MDC
UART7_CTSN_M1 / SPI1_CS1_M1 /	I2C8_SDA_M4 /	GMAC1_MDIO	/	MIPI_TE1	PWM15_IR_M0	GPIO3_C3_d	AM39	GMAC0_MDIO
UART5_TX_M1 /	SPI3_CS0_M3 /	CAN2_RX_M0 / CIF_D8	/	FSPI_CS0N_M2	/	GPIO3_C4_u	AU34	HOST_WAKE_BT_H
UART5_RX_M1 /	SPI3_CS1_M3 /	CAN2_TX_M0 / CIF_D9	/	FSPI_CS1N_M2	/	GPIO3_C5_u	AV34	BT_WAKE_HOST_H
/	SPI3_MISO_M3 /	CIF_D10	/	/	/	GPIO3_C6_u	AV30	MIPI_CAM2_PDN_L
/	SPI3_MOSI_M3 / I2C5_SCL_M0 /	CIF_D11	PCIE20X1_2_CLKREQN_M0 /	HDMI_TX0_SCL_M2	/	GPIO3_C7_u	AU30	PCIE20x1_2_CLKREQn_M0
UART4_RX_M1 /	SPI3_CLK_M3 / I2C5_SDA_M0 /	CIF_D12	PCIE20X1_2_WAKEN_M0 /	HDMI_TX0_SDA_M2	PWM0_M2	GPIO3_D0_u	AW31	WIFI_WAKE_HOST_H
UART4_TX_M1 /	SPI0_MISO_M3 /	CIF_D13	PCIE20X1_2_PERSTN_M0 /		PWM9_M2	GPIO3_D1_d	AY27	PCIE20x1_2_PERSTn_M0
UART9_RTSN_M2 /	SPI0_MOSI_M3 / I2C7_SCL_M2 /	CIF_D14	/		/	GPIO3_D2_d	AY30	UART9_RTSN_M2_BT
UART9_CTSN_M2 /	SPI0_CLK_M3 / I2C7_SDA_M2 /	CIF_D15	/		PWM10_M2	GPIO3_D3_d	AY31	UART9_CTSN_M2_BT
UART9_RX_M2 /	SPI0_CS0_M3 /	MCU_JTAG_TCK_M1	/	HDMI_TX0_HPD_M1	/	GPIO3_D4_d	AV31	UART9_RX_M2_BT
UART9_TX_M2 /	SPI0_CS1_M3 /	MCU_JTAG_TMS_M1	/		PWM11_IR_M3	GPIO3_D5_d	AM30	UART9_TX_M2_BT

RESERVED AF35

VCCIO5_1V8 AF36

VCCIO5_1V8

C1904 100nF X5R 10V C0201

VCC_1V8_S3

R10005 0R 5% R0402

VCCIO5

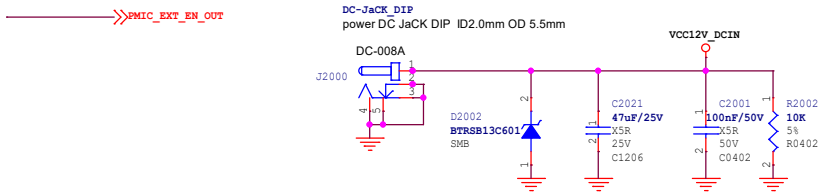
VCCIO5_1 AC33
VCCIO5_2 AC34
C1905 100nF X5R 10V C0201

GMAC0_MCLKINOUT

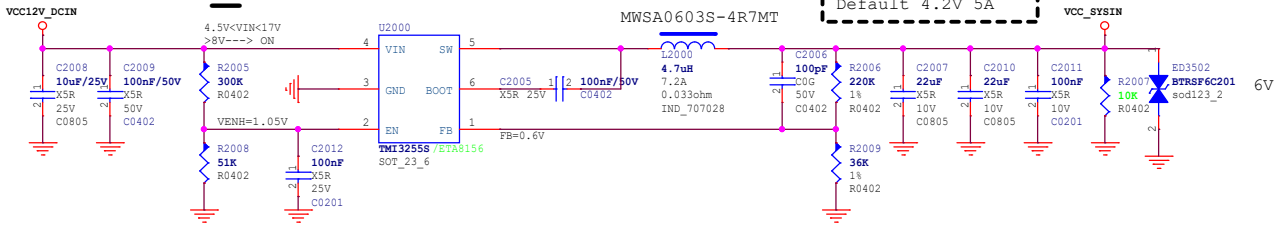
C1908 10pF C0201

SOC_RK3588S

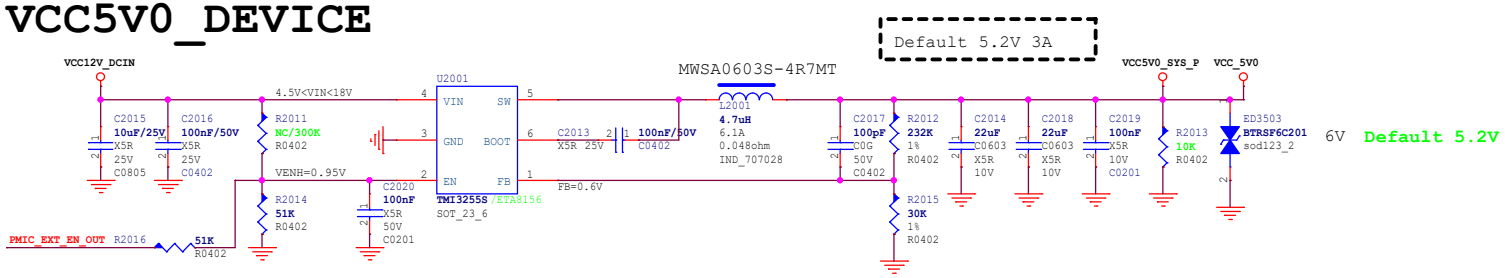
ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	19.RK3588S 1.8V/3.3V GPIO		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	19 of 40



VCC5V0_SYS



VCC5V0_DEVICE



ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	20.Power_IN		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	20 of 40

PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1
PMIC_PWR_CTRL2
PMIC_PWR_CTRL3
PMIC_INT_L
PWRON_L
PMIC_RESET_L
PMIC_EXT_EN_OUT
PMIC_SPI_CLK
PMIC_SPI_CS
PMIC_SPI_MOSI

VCC_SYSIN
ED2200 AZ5825-01F ESD0402

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

VCC_3V3_S3
R2270 2.2K 5% R0402
LED2200 LED_GREEN led_1335qrc POWER_LED
LED2201 LED_GREEN led_1335qrc POWER_LED
R2267 1K R0402 5%
LED_PWM0
R2268 1K 5% R0402
R2269 51K R0402 5%
Q2200 S8050 SOT_23

PMIC RK806-1 BUCK

Default:0.85V
Low frequency:
0.85V-->0.75V

VDD_DDR_S0 Feedback from RK3588S

LPDDR4/4x=1.1V	120K	
LPDDR5=1.05V	110K	

VDD2_DDR_S3

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

VDDQ_DDR_S0

Default:1.8V

VCC1V8_PMU_DDR_S3
VCC_1V8_S3_PLDO6
VCC_1V8_S3

U2200A

BUCK5 2.5A	BUCK1 6.5A	VDD_GPU_S0	Feedback from RK3588S
BUCK6 2.5A	BUCK2 5A	VDD_CPU_LIT_S0	Feedback from RK3588S
BUCK9 2.5A	BUCK3 5A	VDD_LOGIC_S0	Feedback from RK3588S
BUCK8 2.5A	BUCK4 5A	VDD_VDENC_S0	Feedback from RK3588
BUCK10 2.5A	BUCK7 2.5A	VCC_2V0_PLDO_S3	

RK806-1

PMIC RK806-1 Managerment

U2200C
VCCIO
VCCA
RK806-1

RK3588S nPOR
TSADC_SHUT
RK806-1 RESETB
Reset Key

Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

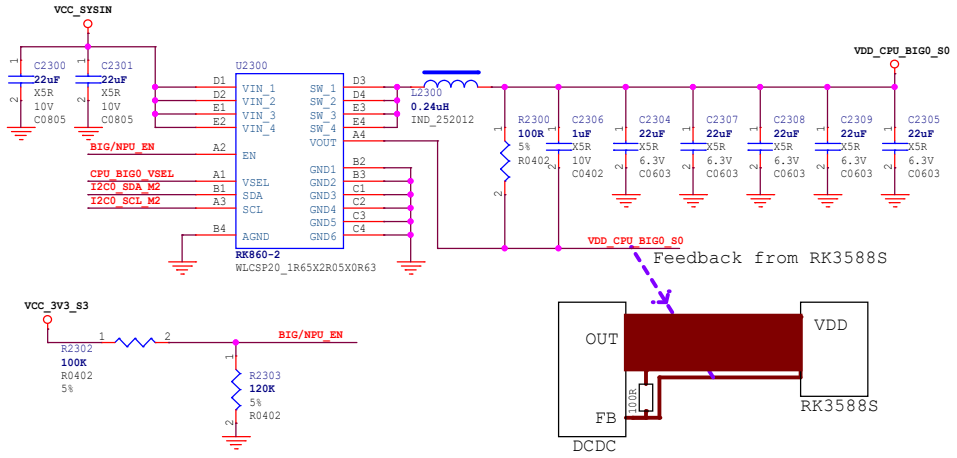
PLDO	VCCA_1V8_S0	Default:1.8V
	VCC_1V8_S0	Default:1.8V
	VDDA_1V2_S0	Default:1.2V
	VCCA_3V3_S0	Default:3.3V
	VCCIO_SD_S0	Default:3.3V
NLDO	VDD_0V75_S3	Default:0.75V
	VDDA_DDR_PLL_S0	Default:0.85V; Low frequency:0.85V-->0.75V
	VDDA_0V75_S0	Default:0.75V
	VDDA_0V85_S0	Default:0.85V
	HDMI_VDDA0V85_S0	Default:0.75V Reserved

VCCA_1V8_S0 R2266 0R 5% R0402 AVDD1V8_DDR_PLL_S0 C2290 1uF X5R 10V C0402

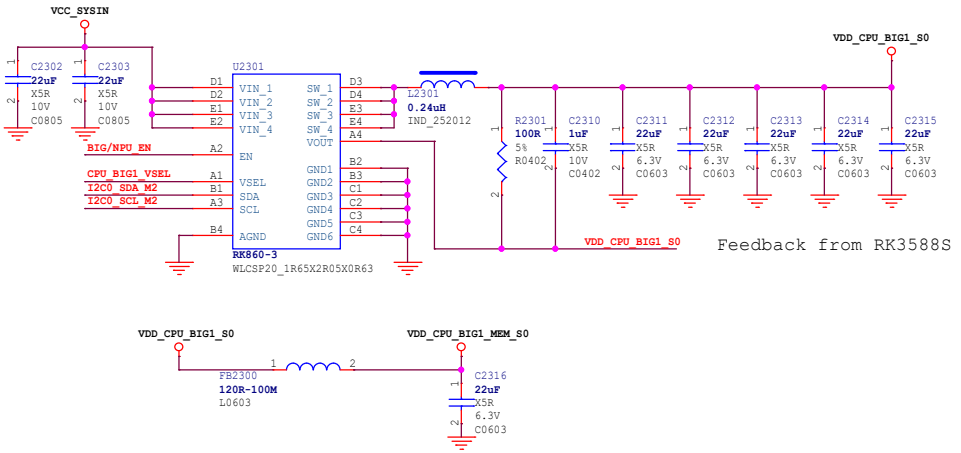
RK806-1

ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	22.Power-PMIC_RK806-1
Date:	Friday, November 14, 2025
Rev:	V1.0
Designed by:	Wang
Sheet:	22 of 40

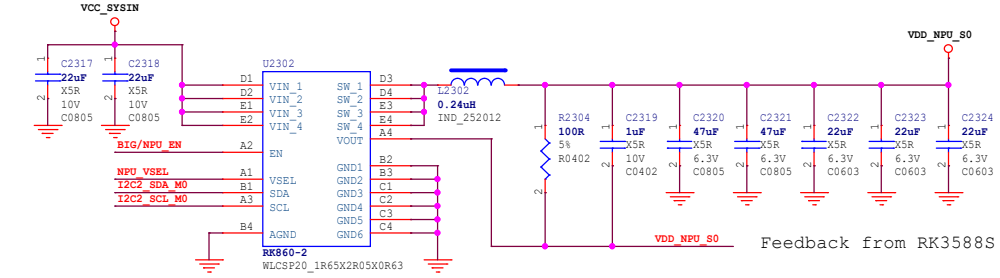
VDD_CPU_BIG0



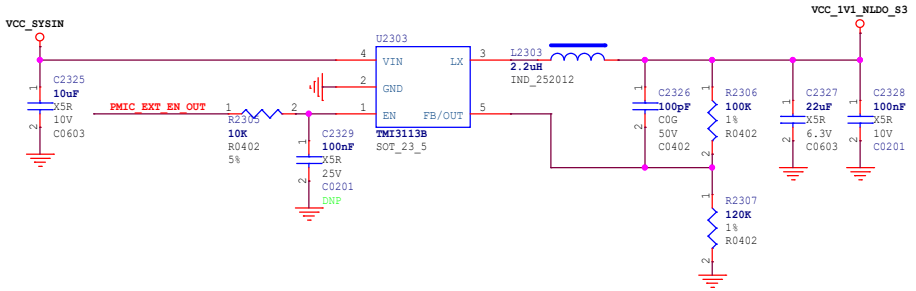
VDD_CPU_BIG1



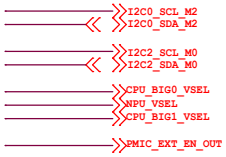
VDD_NPU

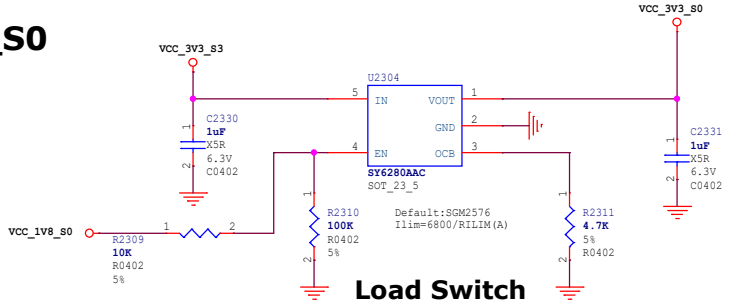


VCC_1V1_NLDO



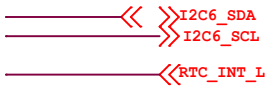
VCC_3V3_S0

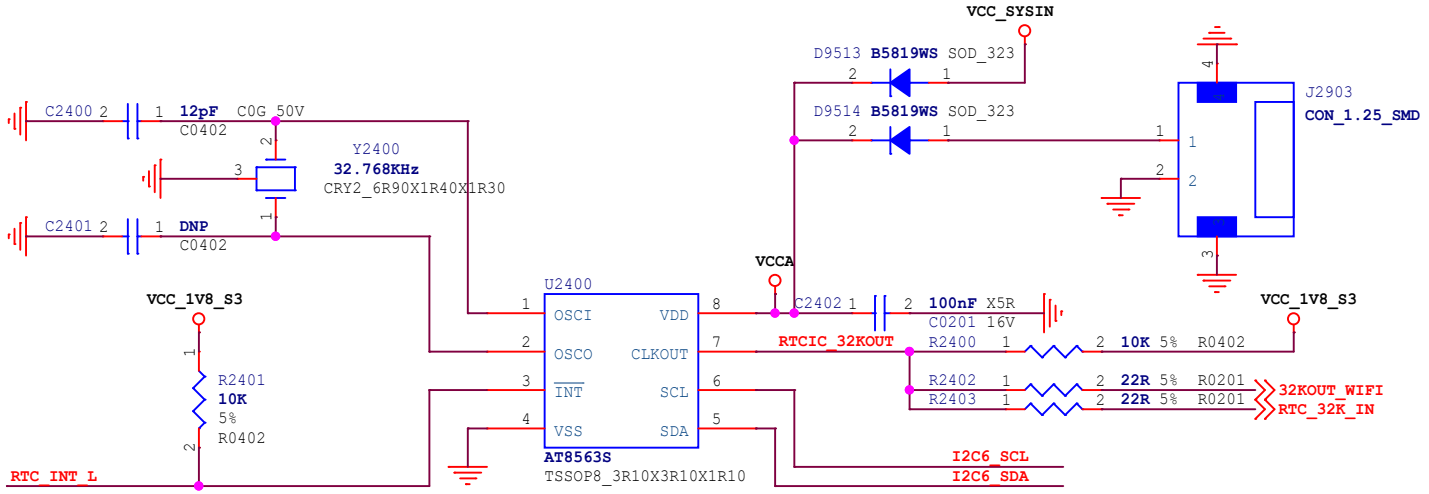




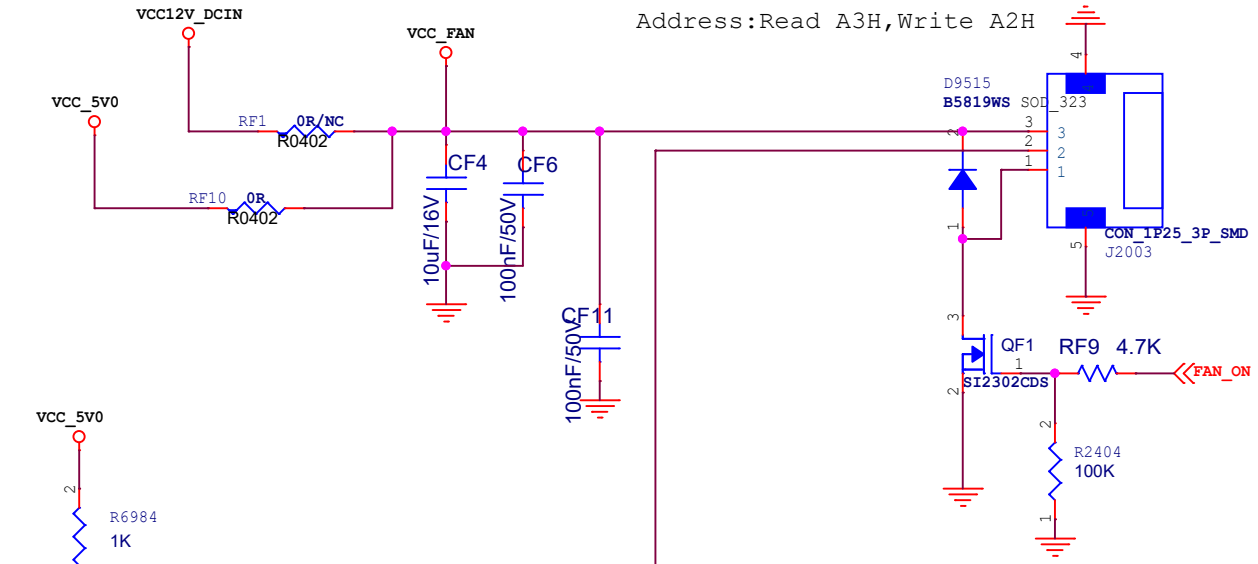
ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	23.Power_Ext Discrete		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	23 of 40

RTC IC

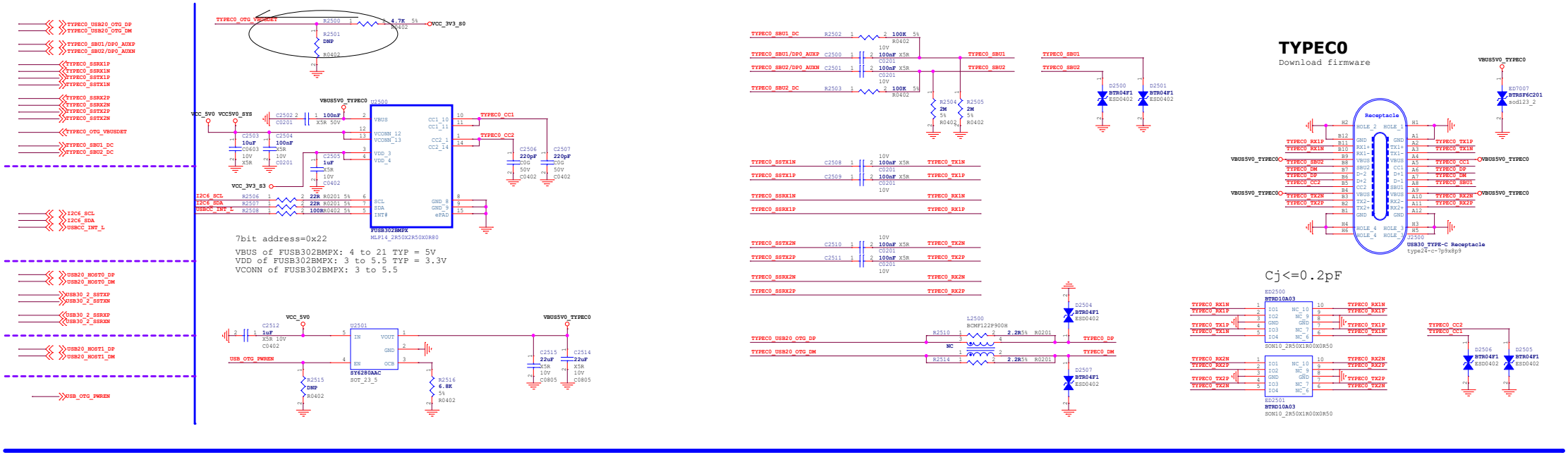


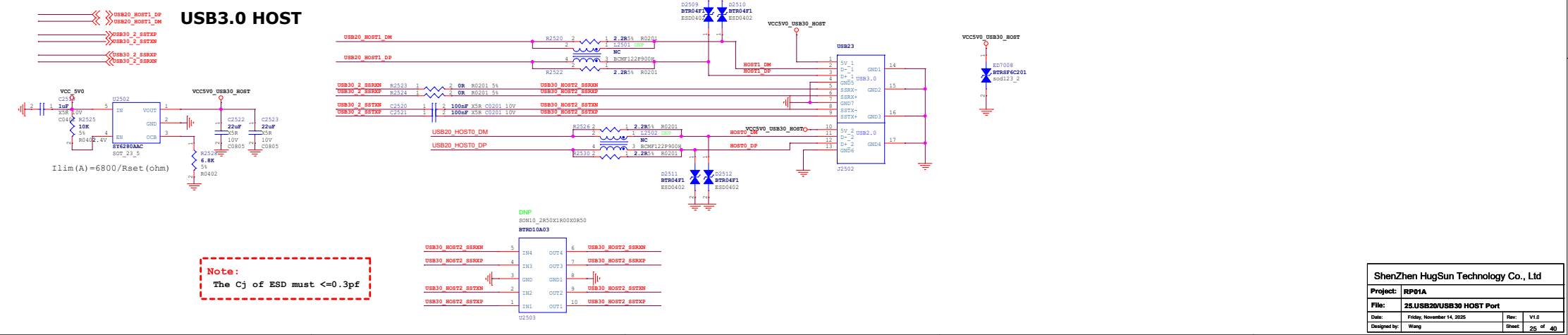


Address:Read A3H,Write A2H



ShenZhen HugSun Technology Co., Ltd			
Project:	**RP01A**		
File:	**24.RTC/FAN**		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	24 of 40





ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	25.USB20/USB30 HOST Port
Date:	Friday, November 14, 2025
Rev:	V1.0
Designed by:	Wang
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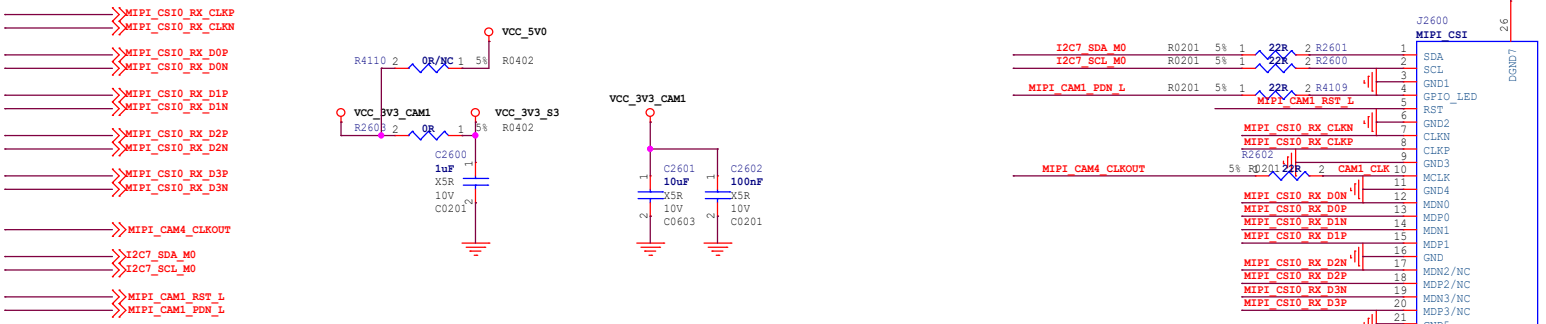
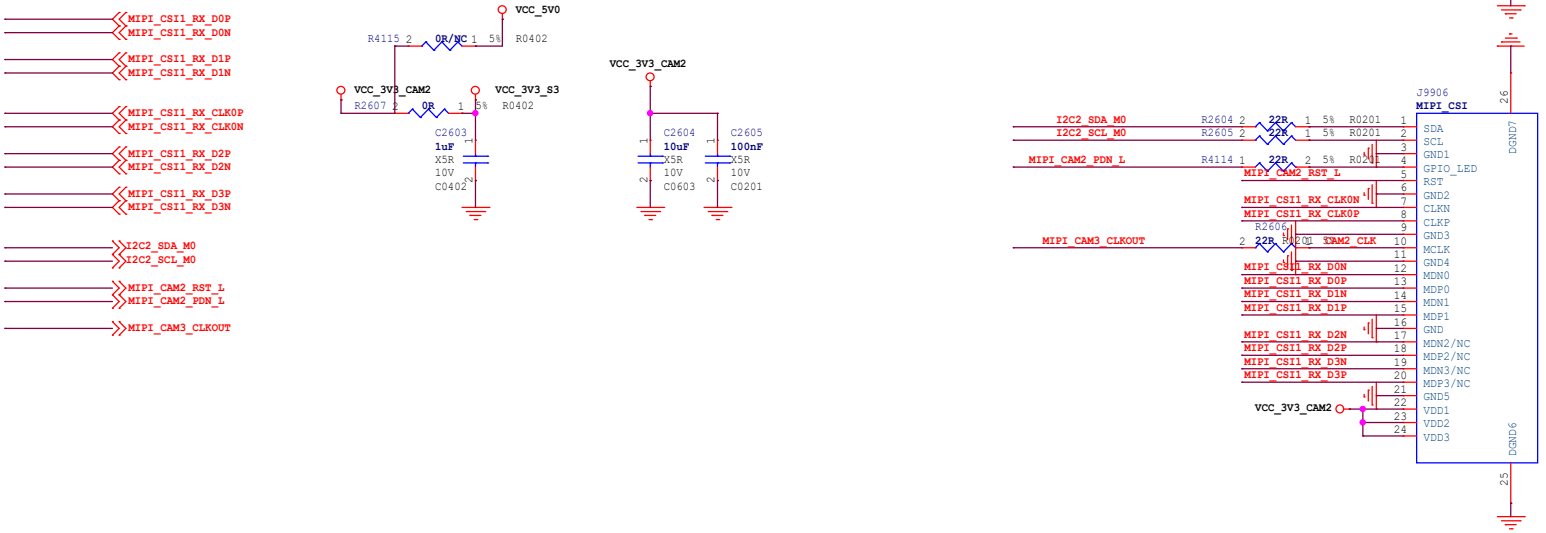
MIPI-DPHY0_RX

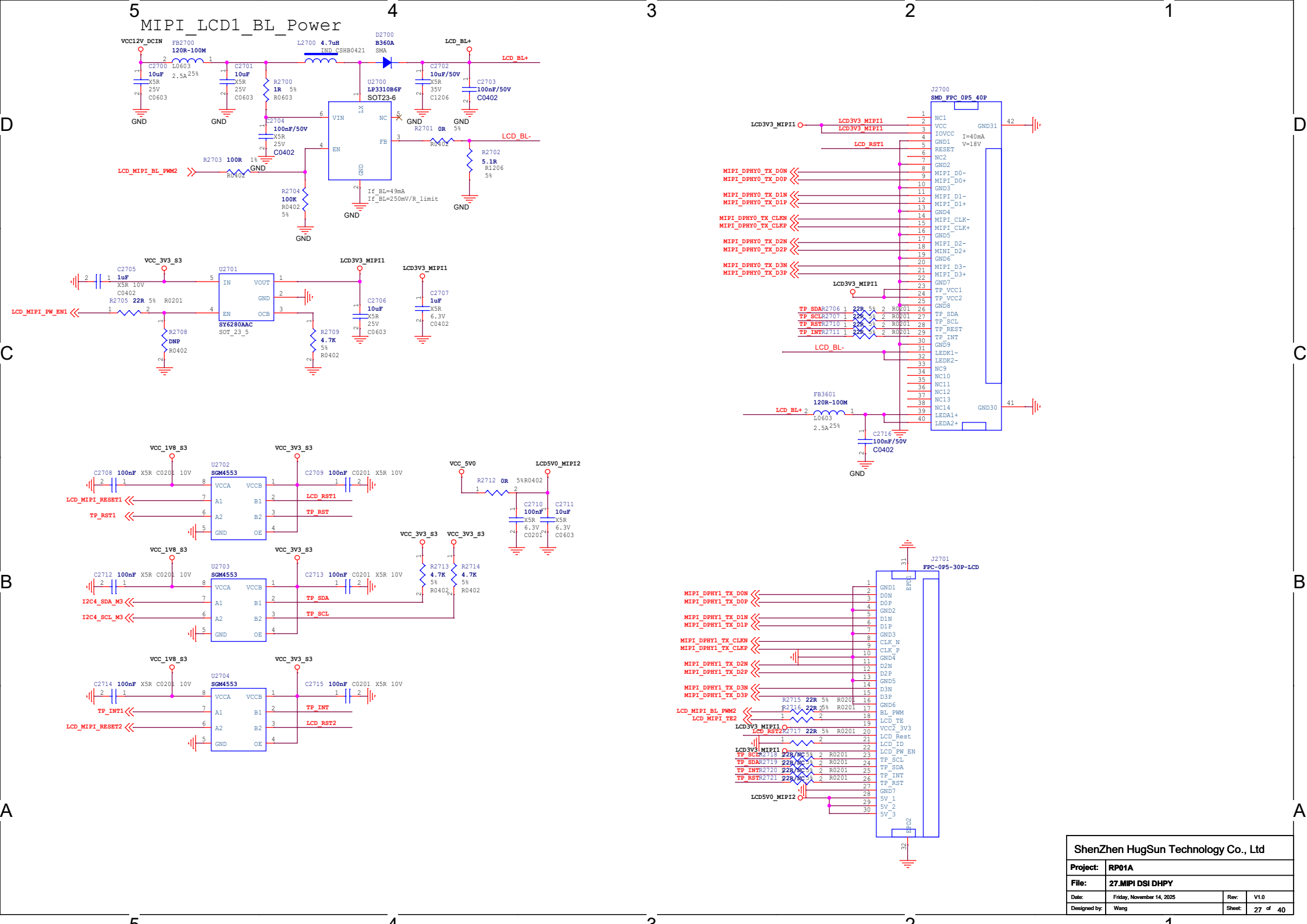


MIPI-DPHY1_RX



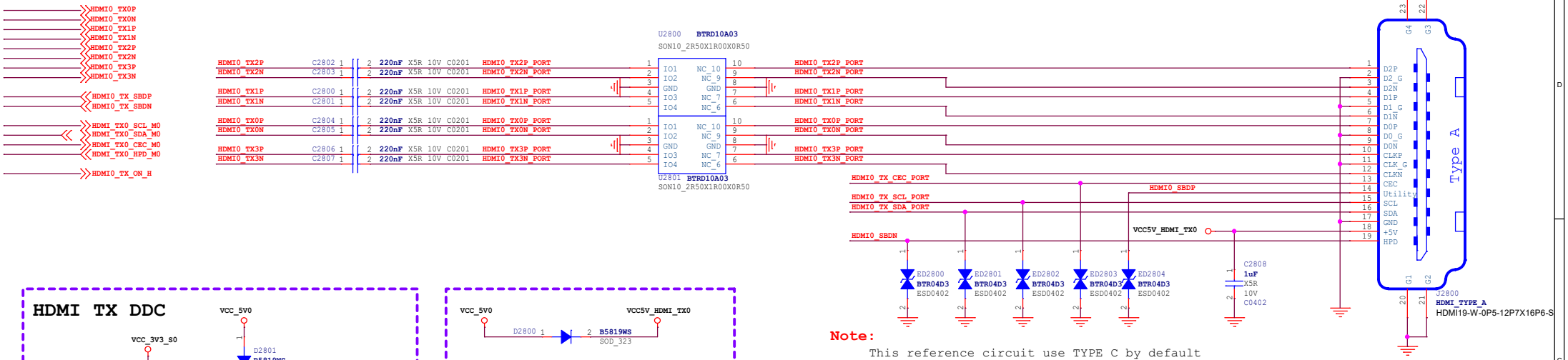
ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	26.CAM MIPI CSI_DPHY-RX		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	26 of 40

MIPI_LCD1_BL_Power

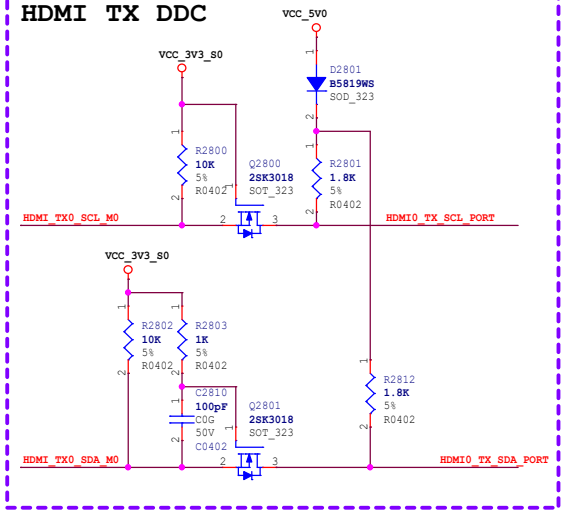


ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	27.MIPI DSI DHPY
Date:	Friday, November 14, 2025
Rev:	V1.0
Designed by:	Wang
Sheet:	27 of 40

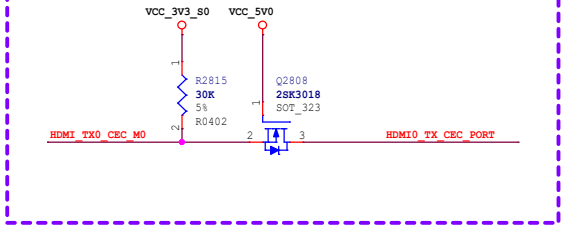
HDMI2.1 TX0

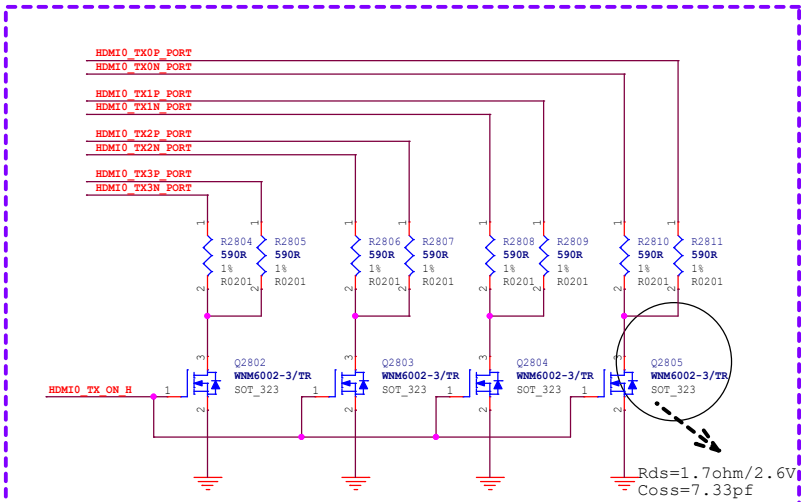


HDMI TX DDC



HDMI TX CEC

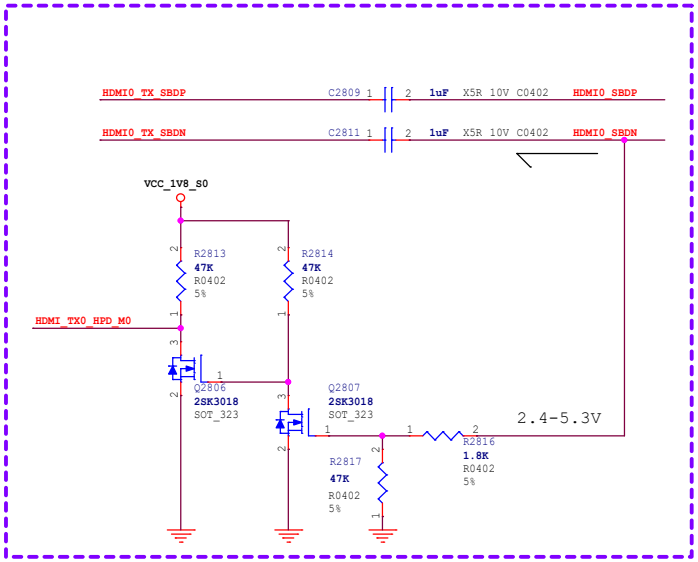




Note:

The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

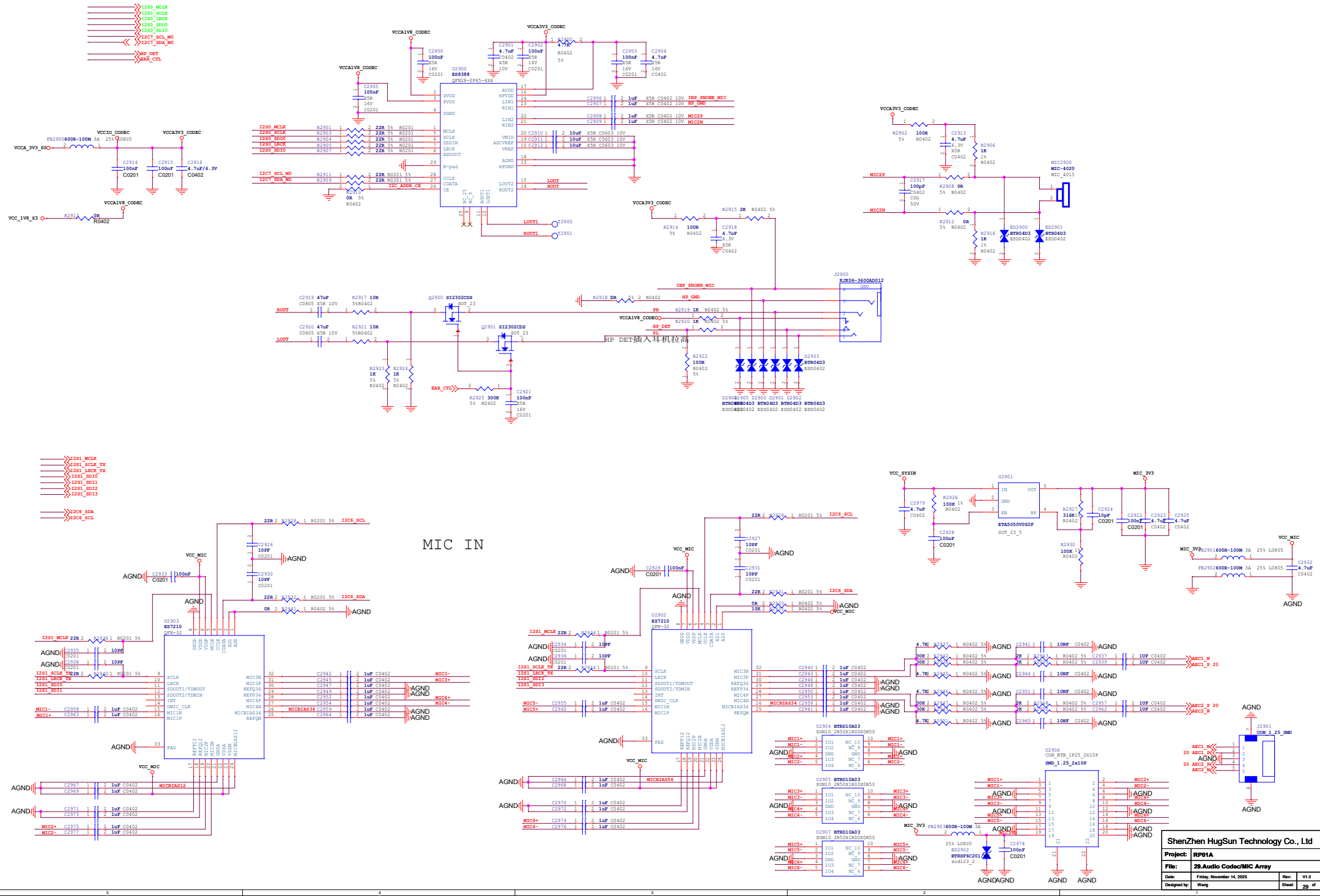


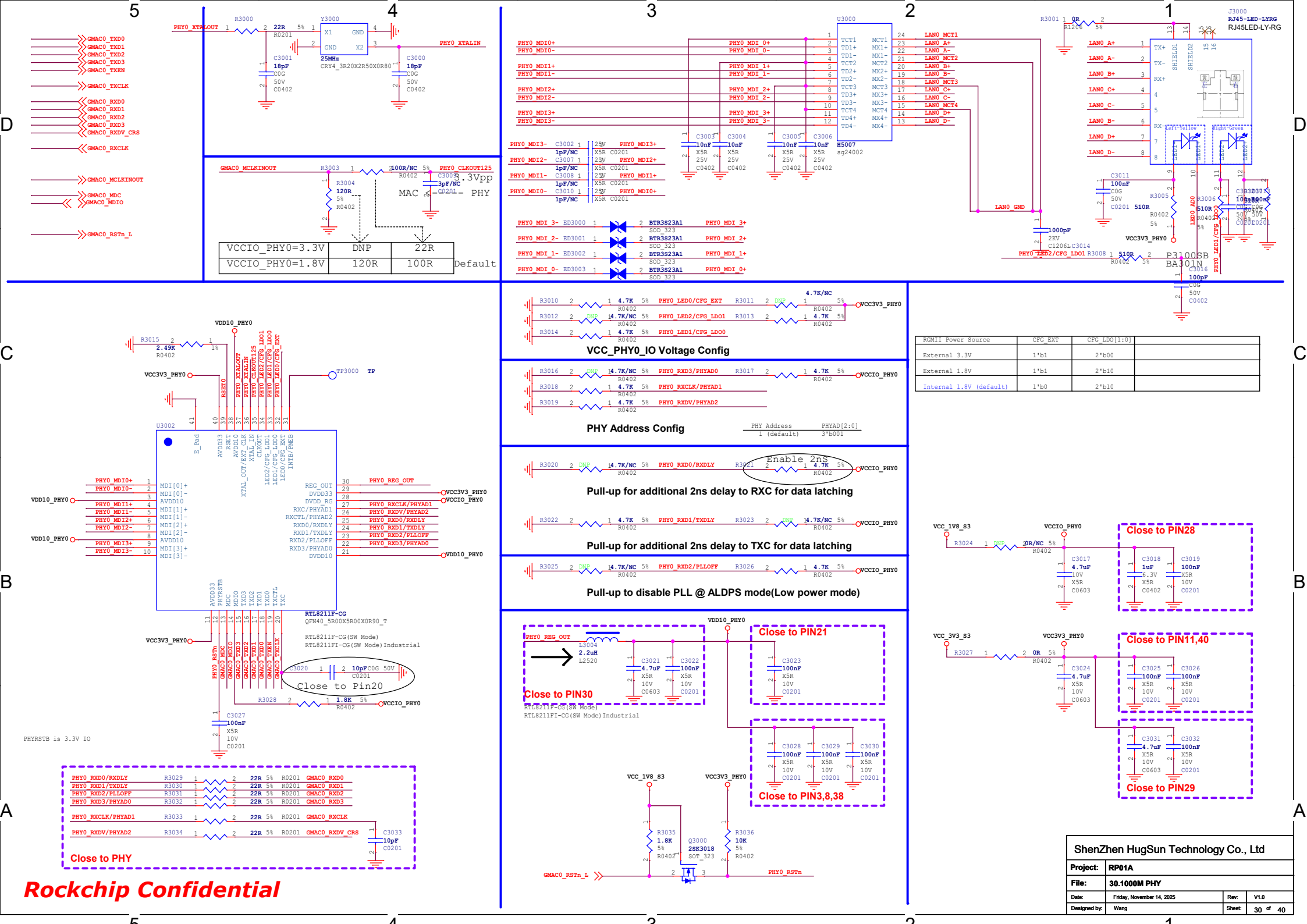
Note:

This reference circuit use TYPE C by default
If the project needs TYPE A, you must replace the library with TYPE A.

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	28.VO-HDMI2.1 TX		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	28 of 40

CODEC


I2S0_MCLK
I2S0_SCLK
I2S0_LRCK
I2S0_SDO0
I2S0_SDI0
I2C7_SCL_M0
I2C7_SDA_M0
HP_DET
EAR_CTL
VCCA1V8_CODEC
VCCA3V3_CODEC
U2900
ES8388
QFN28-0P45-4X4
VCCIO_CODEC
VCC_1V8_S3
LOUT1
ROUT1
LOUT2
ROUT2
INP_PHONE_MIC
HP_GND
MIC2P
MIC2N
I2C_ADDR_CE
J2900
KJK06-3600AD012
Q2900 SI2302CDS
Q2901 SI2302CDS
HP DET插入耳机拉高
MIC IN
U2903
ES7210
QFN-32
U2902
U2904 BTRD10A03
U2905 BTRD10A03
U2907 BTRD10A03
U2906
CON_BTB_1P25_2X10P
SMD_1.25_2x10P
J2901
CON_1_25_SMD
MIC_3V3
VCC_SYSIN
VCC_MIC
ETA5050V0S2F
ShenZhen HugSun Technology Co., Ltd
Project: RP01A
File: 29.Audio Codec/MIC Array
Date: Friday, November 14, 2025
Rev: V1.0
Designed by: Wang
Sheet: 29 of 40


GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_L
PHY0_XTALOUT
R3000
22R
Y3000
25MHz
CRY4_3R20X2R50X0R80
PHY0_XTALIN
C3001
18pF
C0G
50V
C0402
C3000
GMAC0_MCLKINOUT
R3003
100R/NC
PHY0_CLKOUT125
C3009
3pF/NC
C0201
3.3Vpp
MAC
PHY
R3004
120R
R0402
VCCIO_PHY0=3.3V
DNP
22R
VCCIO_PHY0=1.8V
120R
100R
Default
PHY0_MDI0+
PHY0_MDI0-
PHY0_MDI1+
PHY0_MDI1-
PHY0_MDI2+
PHY0_MDI2-
PHY0_MDI3+
PHY0_MDI3-
U3000
H5007
sg24002
C3002
C3007
C3008
C3010
1pF/NC
X5R
C0201
ED3000
ED3001
ED3002
ED3003
BTR3S23A1
SOD_323
LAN0_MCT1
LAN0_A+
LAN0_A-
LAN0_MCT2
LAN0_B+
LAN0_B-
LAN0_MCT3
LAN0_C+
LAN0_C-
LAN0_MCT4
LAN0_D+
LAN0_D-
LAN0_GND
1000pF
2KV
C1206L
C3014
R3001
0R
R1206
J3000
RJ45-LED-LYRG
RJ45LED-LY-RG
SHIELD1
SHIELD2
LED1
LED2
Left-Yellow
Right-Green
C3011
100nF
R3005
510R
R3006
LED0_ADO
LED1/CFG
VCC3V3_PHY0
P3100SB
BA301N
C3016
100pF
VDD10_PHY0
R3015
2.49K
TP3000
TP
U3002
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
RSET0
PHY0_XTALOUT
PHY0_XTALIN
PHY0_CLKOUT125
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
PHY0_LED0/CFG_EXT
E_Pad
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
PHY0_RSTn
GMAC0_MDC
GMAC0_MDIO
GMAC0_TXD3
GMAC0_TXD2
GMAC0_TXD1
GMAC0_TXD0
GMAC0_TXEN
GMAC0_TXCLK
C3020
10pF
C0G
50V
C0201
Close to Pin20
R3028
1.8K
VCCIO_PHY0
C3027
100nF
PHYRSTB is 3.3V IO
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
R3029
R3030
R3031
R3032
R3033
R3034
22R
R0201
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXCLK
GMAC0_RXDV_CRS
C3033
10pF
Close to PHY
R3010
R3012
R3014
4.7K
4.7K/NC
DNP
PHY0_LED0/CFG_EXT
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
R3011
R3013
VCC_PHY0_IO Voltage Config
R3016
R3018
R3019
PHY0_RXD3/PHYAD0
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY Address Config
PHY Address
PHYAD[2:0]
1 (default)
3'b001
R3020
R3021
PHY0_RXD0/RXDLY
Enable 2ns
Pull-up for additional 2ns delay to RXC for data latching
R3022
R3023
PHY0_RXD1/TXDLY
Pull-up for additional 2ns delay to TXC for data latching
R3025
R3026
PHY0_RXD2/PLLOFF
Pull-up to disable PLL @ ALDPS mode(Low power mode)
L3004
2.2uH
L2520
PHY0_REG_OUT
C3021
4.7uF
C3022
100nF
Close to PIN30
C3023
Close to PIN21
C3028
C3029
C3030
Close to PIN3,8,38
VCC_1V8_S3
VCC3V3_PHY0
R3035
1.8K
R3036
10K
Q3000
2SK3018
SOT_323
GMAC0_RSTn_L
PHY0_RSTn
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V
1'b1
2'b00
External 1.8V
2'b10
Internal 1.8V (default)
1'b0
VCC_1V8_S3
R3024
20R/NC
C3017
4.7uF
C3018
1uF
6.3V
C3019
Close to PIN28
VCC_3V3_S3
R3027
0R
C3024
C3025
C3026
Close to PIN11,40
C3031
C3032
Close to PIN29
Rockchip Confidential
ShenZhen HugSun Technology Co., Ltd
Project:
RP01A
File:
30.1000M PHY
Date:
Friday, November 14, 2025
Rev:
V1.0
Designed by:
Wang
Sheet:
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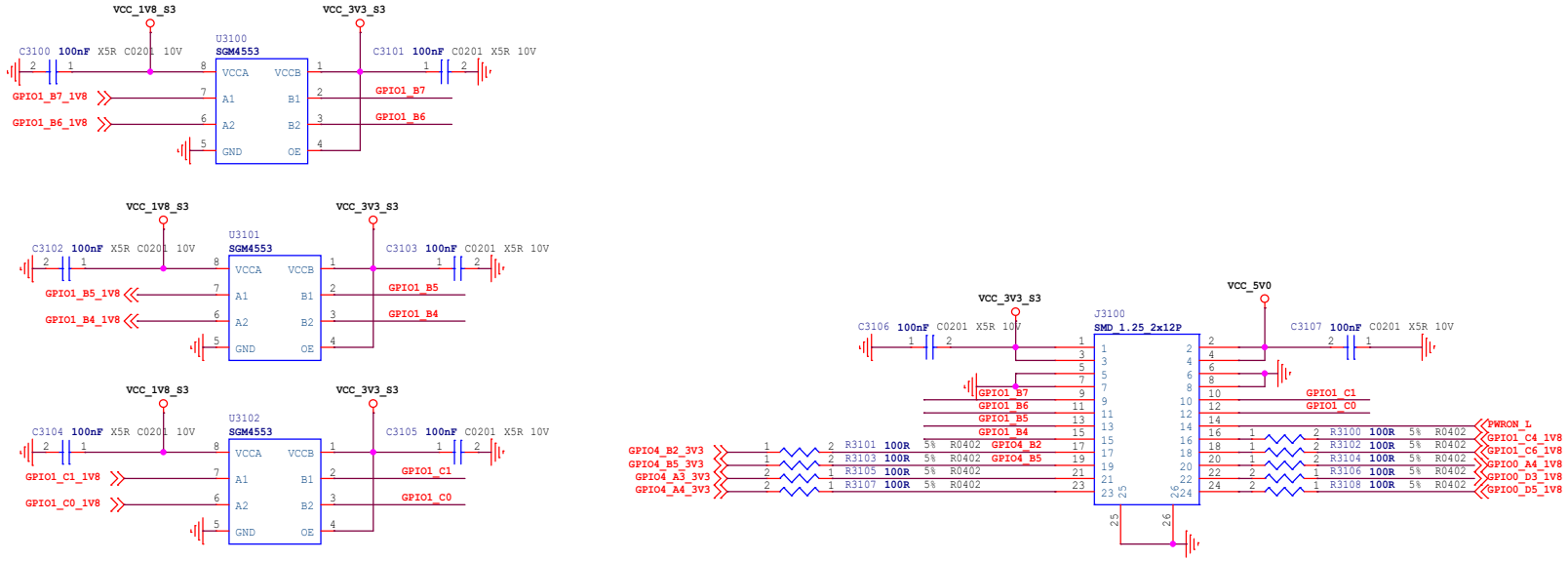
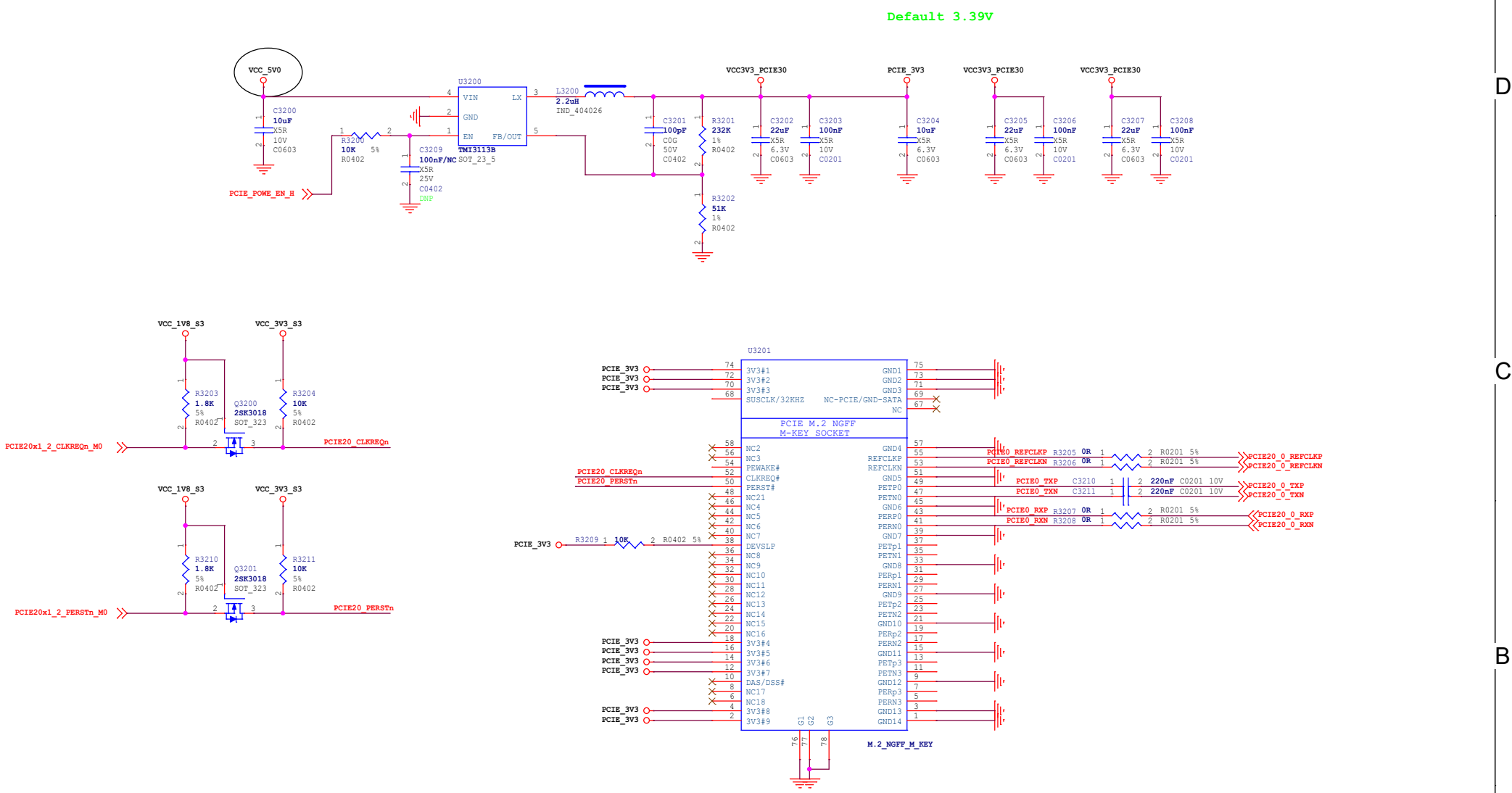
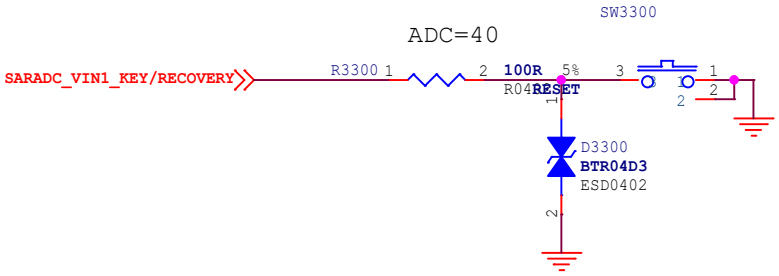


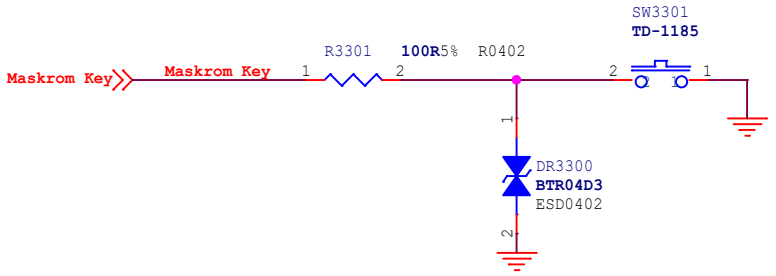
ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	31.CON_IO		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	31 of 40



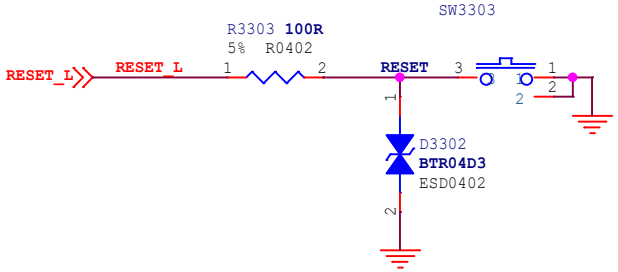
ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	32.M-key PCIE
Date:	Friday, November 14, 2025
Rev:	V1.0
Designed by:	Wang
Sheet:	32 of 40



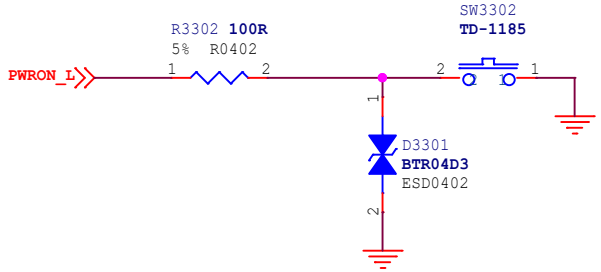
Maskrom Key



Reset_Key

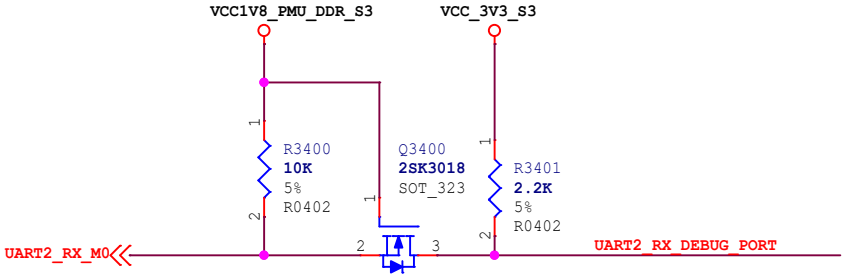


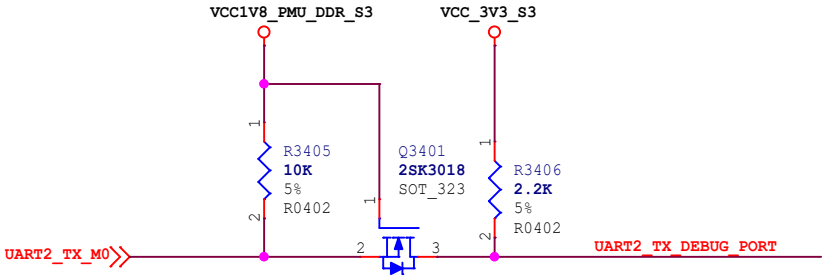
PWR_Key

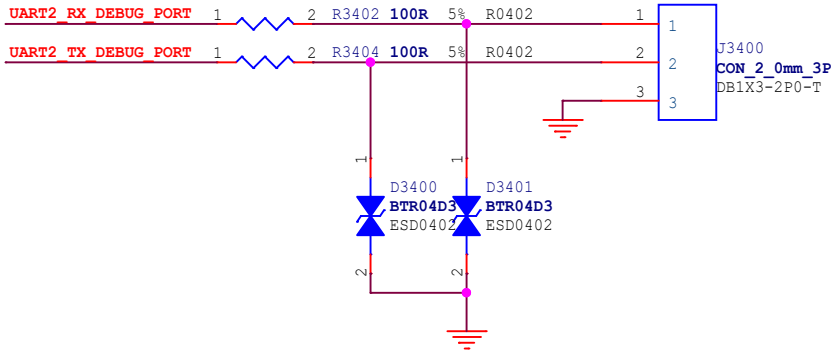


ShenZhen HugSun Technology Co., Ltd			
Project:	**RP01A**		
File:	**33.KEY Array**		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	33 of 40

UART Debug

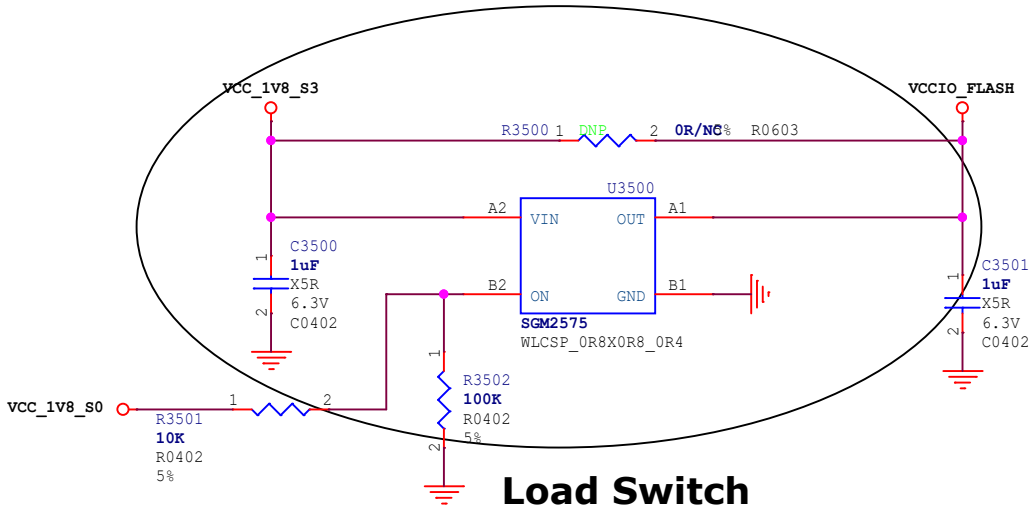






ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	34.UART Debug		
Date:	Friday, November 14, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	34 of 40

SPI FLASH



Load Switch

ShenZhen HugSun Technology Co., Ltd			
Project:	**RP01A**		
File:	**35.Flash-SPI FLASH(opt)**		
Date:	Friday, November 14, 2025	Rev:	V1.0
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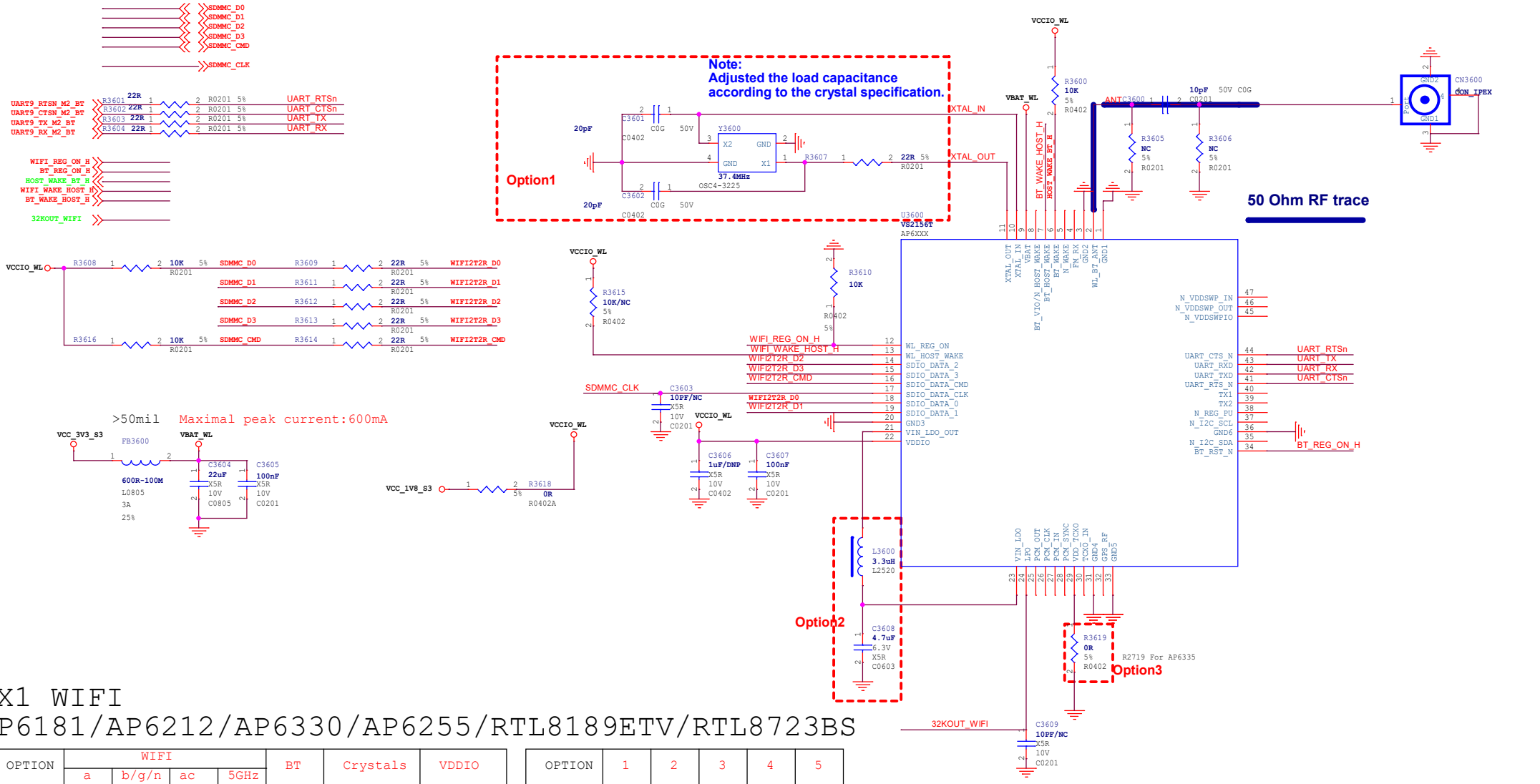
MicroSD Card



1X1 WIFI
AP6181/AP6212/AP6330/AP6255/RTL8189ETV/RTL8723BS

OPTION	WIFI				BT	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181	No	Yes	No	No	No	26MHz	1.71-3.6V
AP6212	No	Yes	No	No	Yes	26MHz	1.71-3.6V
AP6330	Yes	Yes	No	Yes	Yes	26MHz	1.2-2.9V
AP6255 AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V
RTL8189ETV	No	Yes	No	No	No	40MHz On the module	3.3V
RTL8723BS	No	Yes	No	No	Yes	On the module	3.3V

OPTION	1	2	3	4	5
AP6181	Yes	Yes	No		
AP6212	Yes	Yes	No		
AP6330	Yes	Yes	No		
AP6335 AP6255	Yes	Yes	Yes		
RTL8189ETV MODULE	No	No	No		
RTL8723BS	No	No	No		

Default:AP6255

Note:
Yes:框内要贴
No:框内不贴

ShenZhen HugSun Technology Co., Ltd			
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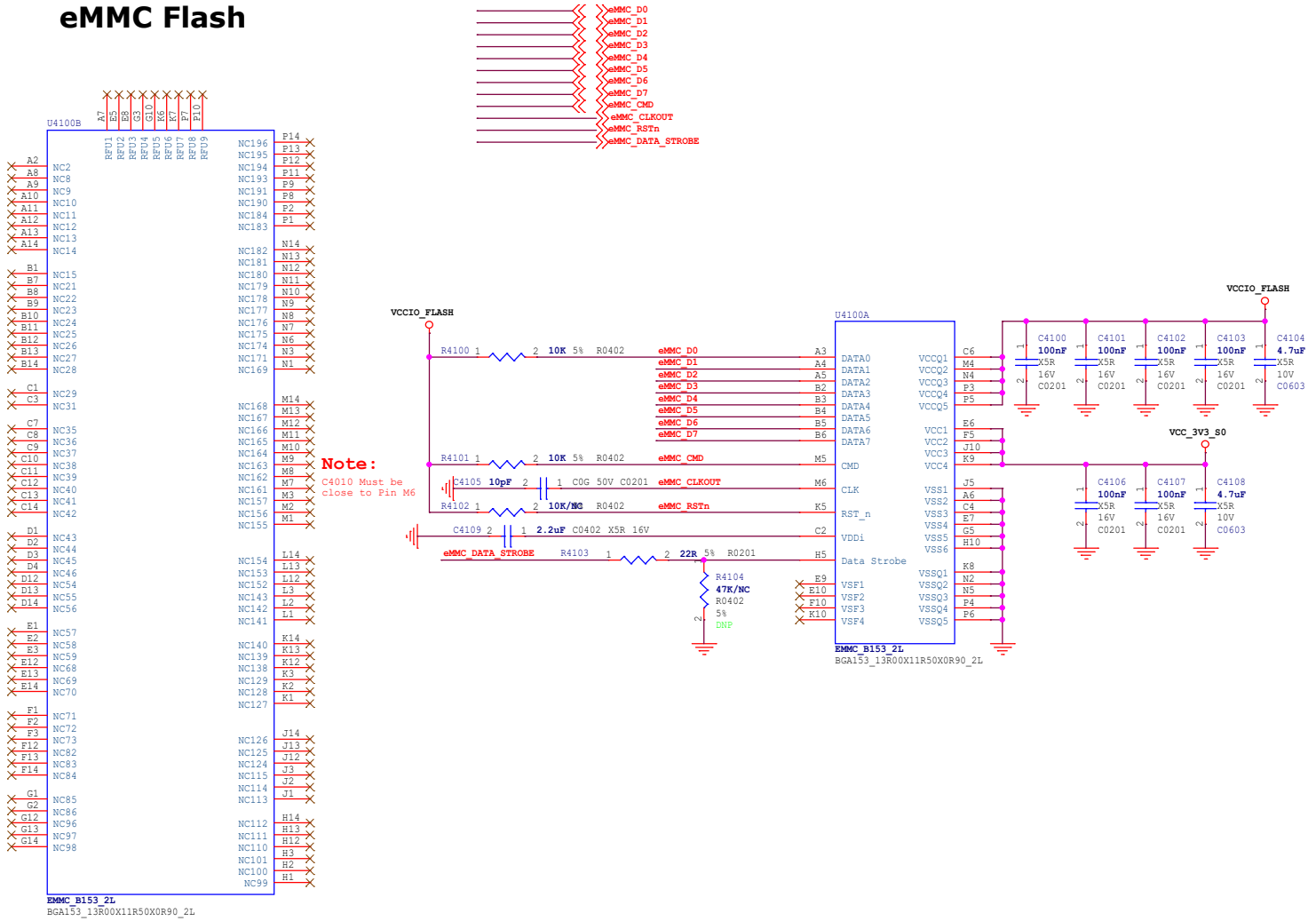
eMMC Flash



ShenZhen HugSun Technology Co., Ltd	
Project:	RP01A
File:	37.EMMC
Date:	Friday, November 14, 2025
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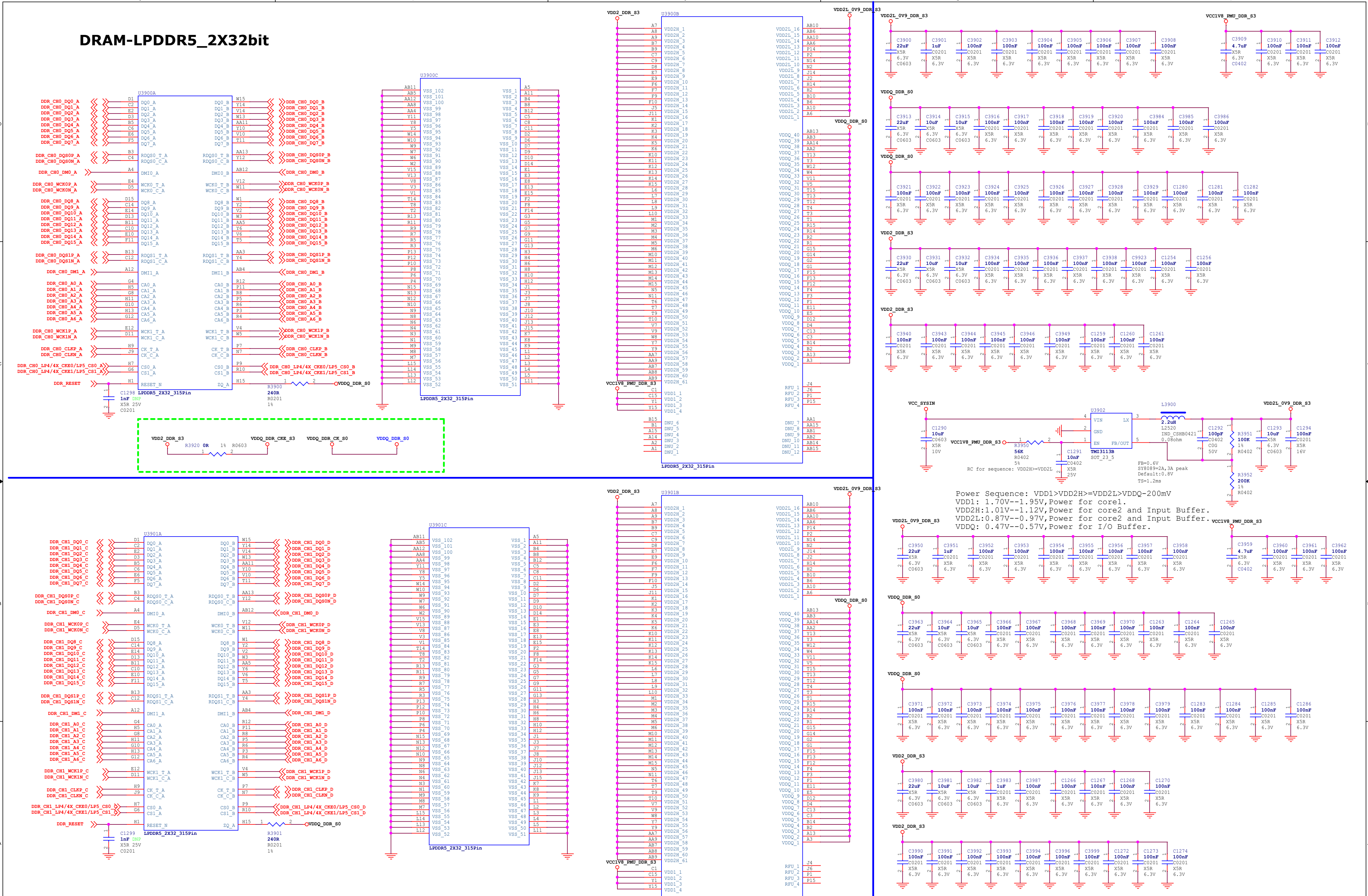

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Project:	RP01A
File:	38.DRAM-LPDDR5_2X32bit
Date:	Friday, November 14, 2025
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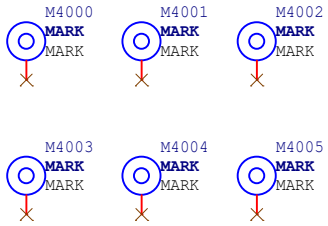
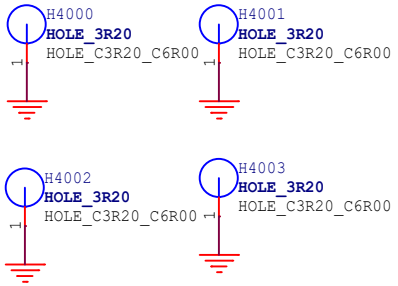
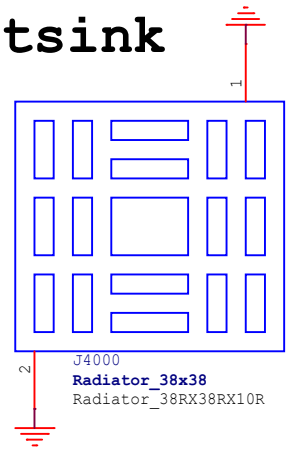
PCB Mark Point



Mechanical Hole



Heatsink



Shield

ShenZhen HugSun Technology Co., Ltd			
Project:	RP01A		
File:	40.Mark/Heatsink		
Date:	Monday, November 17, 2025	Rev:	V1.0
Designed by:	Wang	Sheet:	40 of 40